Winter – 2009-10

EE214 - Design Project

WIDEBAND TRANSIMPEDANCE AMPLIFIER DESIGN

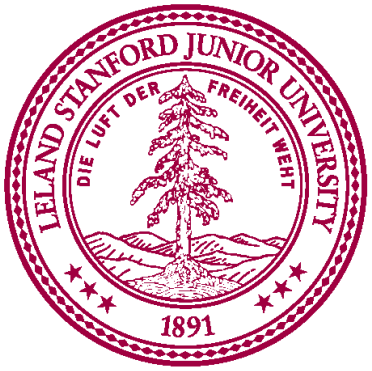
Submitted by

Piyush Keshri (0559 4497)

Aditi Goyal (0559 1220)

On

March 10th, 2010



PART 1 – Analysis and completion of a SiGe BJT baseline design

a) & b) Bias Point Calculations

Results for Operating point voltages, Gm and Rμ calculations are as follows:

1.1.1 Operating Point Analysis

Node	Hand Analysis	Spice Results	% Error
VB	0.8V	0.784V	2.04
VBH	1.6V	1.4725V	8.66
VBB	2V	1.9938V	0.31
V1a,V1b	2V	2.0083V	-0.41
Via,Vib	1.2V	1.2106V	-0.88
V2a,V2b	2V	2.0013V	-0.06
Voa,Vob	1.2V	1.2175V	-1.43
Vx	1.2V	1.2247V	-2.02

1.1.2 Gm Measurements

Transistor	Hand Analysis	Spice Results	% Error
Q1a,Q1b	19.23e-3	17.684e-3	8.74
Q2a,Q2b	19.23e-3	17.684e-3	8.74
Q3a,Q3b	19.23e-3	17.684e-3	8.74

1.1.3 r_π Measurements

Transistors	Hand Analysis	Spice Results	% Error
Q1a,Q1b	15.04K	14.58K	3.155
Q2a,Q2b	15.04K	14.58K	3.155
Q3a,Q3b	15.04K	14.58K	3.155

c) Mid band loop gain (T_o) Analysis

The given circuit consists of a (transimpedance gain) → (common base stage) (Differential Amplifier stage) (Common Collector) topology. Taking the respective gains of each stage the following formula for Loop gain can be easily deduced:

$$T_o = \left(\frac{1}{g_{m1} + \frac{1}{R_{fb}}}\right)(g_{m1}R_{1a})(g_{m2}R_{2a})\left(\frac{R_L||R_f}{\frac{1}{g_{m3}} + R_L||R_f}\right)\frac{1}{R_f}$$

Using the values from the table above, we obtain $\boldsymbol{T_o = 14.44\,\Omega}$ and $\boldsymbol{a_o = 14.44\,k\Omega}$

Thus, the overall transimpedance of the closed loop system becomes,

$$A_O = \frac{2a_o}{(1 + a_o f)}$$

Using the values determined above,

Transimpedance Gain (low frequency), A_O = 28.470 kΩ

d) Open Loop poles hand Analysis

The three significant poles of the circuit can be easily identified as coming from the points Via, V1a and V2a. The dominant pole (p_1) of the system will be determined by the high capacitance Cpa at node Via. The corresponding poles are given as follows:

$$P_1 = \frac{1}{(R_f || \frac{1}{g_{m1a}})(C_{pa} + 2C_\mu + C_\pi)} = 1.53GHz$$

$$P_2 = \frac{1}{2\pi(R_{1b}||r_\pi)(C_\pi + C_\mu + C_p(1 + g_{m2}R_{2a}))} = 1.778G\text{□□}Hz$$

$$P_3 = \frac{1}{2\pi(R_{2a}|| \frac{r_\pi}{(1 - A_3)})(C_\pi{}' + C_\mu{}' + C_p)} = 52.837GHz$$

The values used in the above formulas are as follows:

$C_\pi \cong C_b + 2C_{je0} = 23.288fF$, $C_b = \tau_f g_m = 10.768fF$, $2C_{je0} = 12.52fF$, $C_{pa} = 2pF$

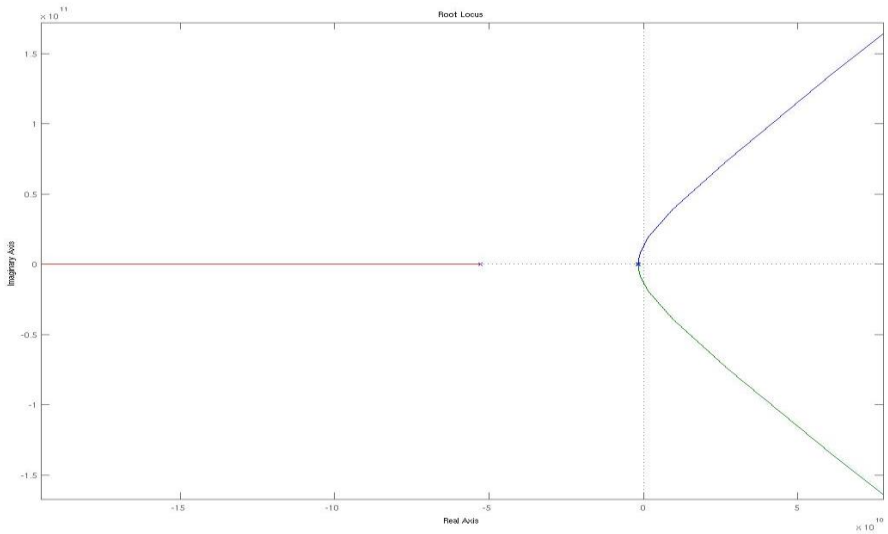
$$C_\mu = \frac{2C_{\mu 0}}{(1 + \frac{V_{CB}}{\Psi_o})^n} = 6.84fF$$

$$C_\mu{}' = C_\mu(1 - \frac{1}{g_m R_2})$$

$$C_\pi{}' = \frac{C_\pi}{1 + g_m(R_F||R_L)}$$

e) Root Locus Plot

Using the open loop poles of the loop gain calculated above, the following root locus plot was generated:



Observation: The root locus plot clearly indicates that the poles of the given closed loop system for the required T_o=14.44 are on the Left Half Plane, and hence, the system is stable.

Determining Closed Loop Poles

To find the closed poles we solved the following equation for To=14.44 using Mathematica:

$$\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)+T_o=0$$

The roots of this equation were:

ω_{p1} = (-1.27+j6.31)e9 rad/s

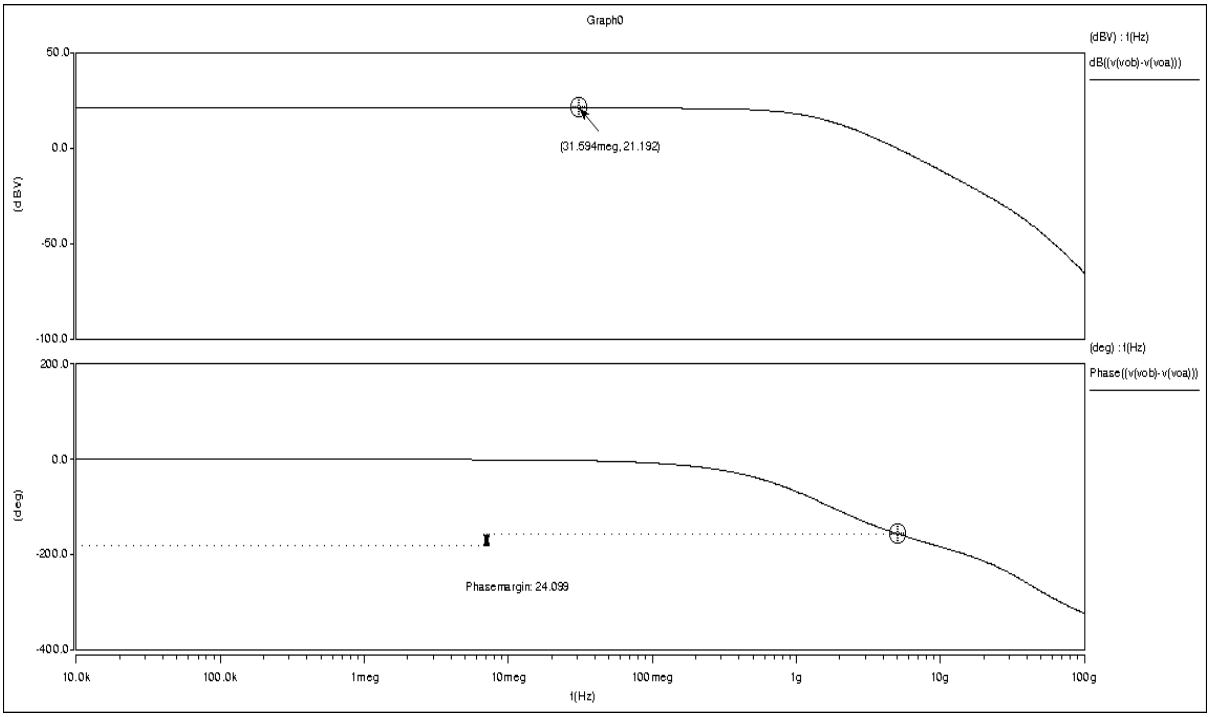
ω_{p2} = (-1.27 – j6.31)e9 rad/s

ω_{p3} = -53.6e9 rad/s

Observation: Since all the poles lie in the LHP, the system is stable. Peaking can occur even in a stable system. The way to predict peaking in the closed loop response is to look at the open loop phase margin which should be more than 60°.

The angle of the dominant complex conjugate poles is 78.62°. Since, the angle of the dominant complex conjugate poles is higher than the 45°, hence3 peaking will occur in the closed loop response of the system.

f) **Open loop bode plots**



SPICE Results Obtained

To = 11.471 (Simulated)
To = 14.44 (Estimated)
% Error (ΔTo) = To (Estimated) – To (Simulated)/ To (Simulated)
= **26.88 %**

Phase Margin, **ϕM = 24.1°**

g) Pole-Zero (pz) Analysis for Loop Gain

Poles and zeroes obtained for the open loop system from SPICE results are as follow:

p_1= -1.49 GHz
p_2= - 1.63GHz
p_3= - 47.02GHz

These results compare well with our hand calculated values of *1.53Ghz, 1.778Ghz and 52.84GHz* respectively.

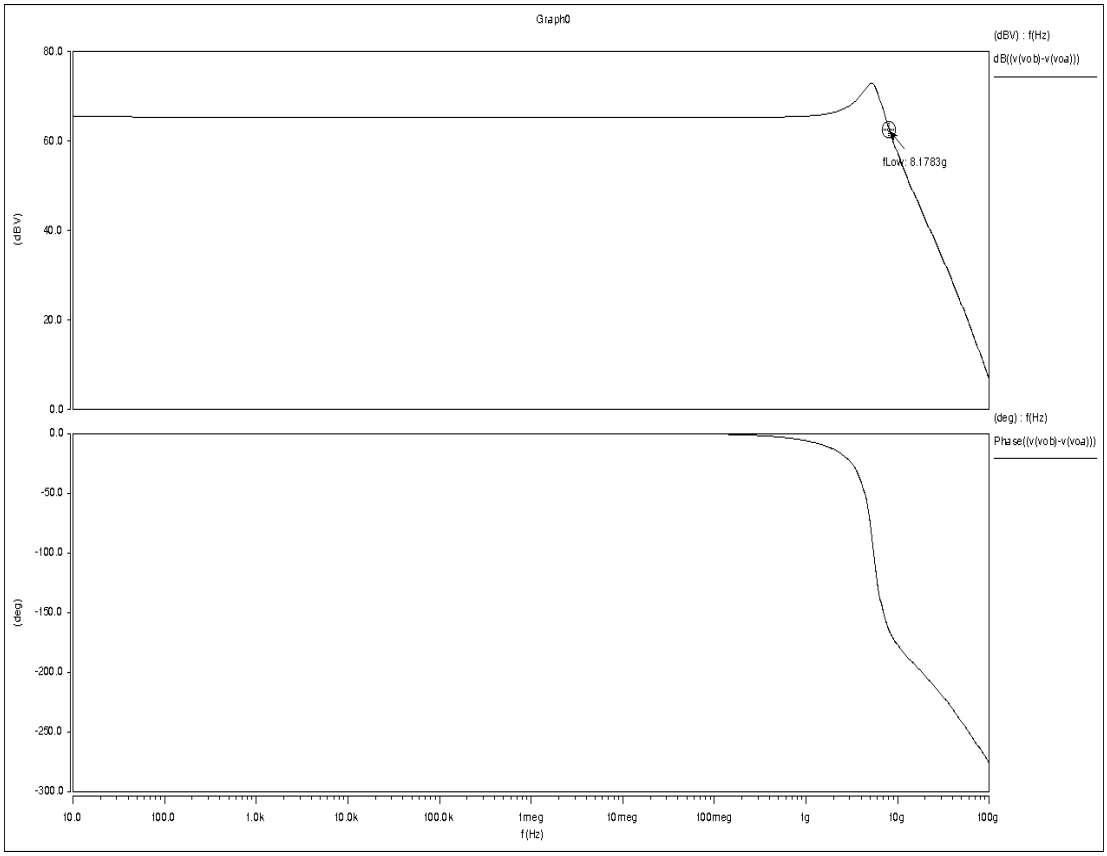
1.5.1 Open Loop Pole Comparison

Hand Calculation	SPICE Results	% Error
P_1 = -1.53 GHz	P_1 = -1.49 GHz	2.68 %
P_2 = -1.778 GHz	P_2 = -1.63 GHz	9.08 %
P_3 = -52.84 GHz	P_3 = -47.02 GHz	12.38 %

Observation: Clearly, SPICE results match the Hand calculations within the range of ~ 10% error.

h) Closed Loop Simulation Results

Bandwidth, $\omega_{3db} = 8.178\ Ghz$
Gain, $A_O = 65.6\ db$



Poles obtained for Closed Loop System from pz Analysis are:

ω_{pc1} = (-1.159+j5.34) GHz

ω_{pc2} = (-1.159-j5.34) GHz

ω_{pc3} = -47.893 GHz

Closed Loop Pole Comparison

Hand Calculation	SPICE Results	% Error
ω_{pc1} = (-1.159+j5.34) GHz	ω_{pc1} = (-1.27+j6.31) GHz	17.8 %
ω_{pc2} = (-1.159-j5.34) GHz	ω_{pc2} = (-1.27+j6.31) GHz	17.8 %
ω_{pc3} = -47.893 GHz	ω_{pc3} = -53.6GHz	10.65 %

Observation: The SPICE results match the Hand calculations within 20% tolerance.

i) Phantom Zero Compensation

Phantom zero compensation have been utilised to improve the phase margin of the loop gain and to improve the stability of the design by introducing a zero in left half plane. The formula utilised to determine the capacitive feedback to be added is as follows:

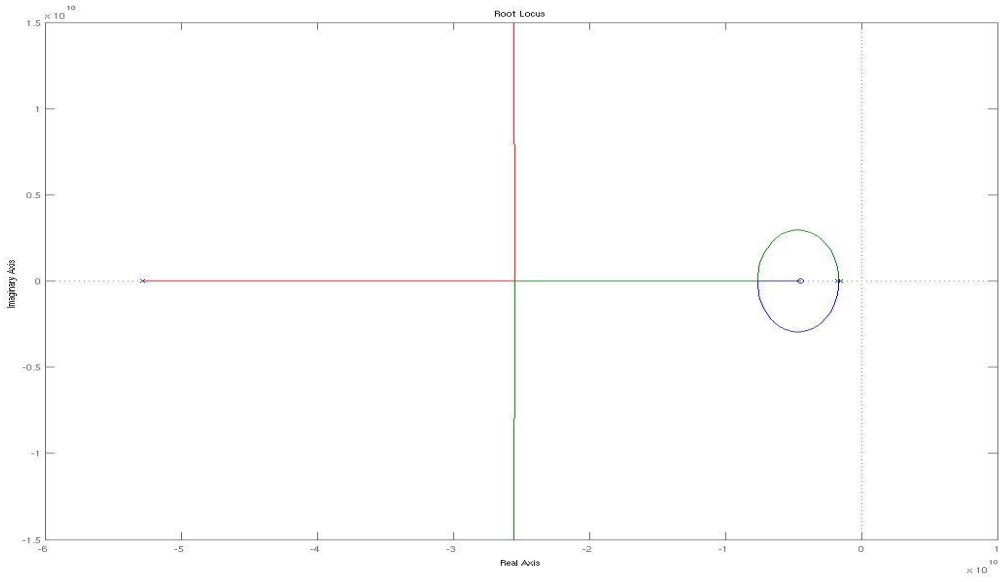
$$T_o = \frac{2\|Z_f\|^2}{\|p_2\|\|p_1\|}$$

$$\text{Where } Z_f = \frac{1}{2\pi R_f C_f}$$

This gives $\underline{C_f = 35.9\ fF}$.

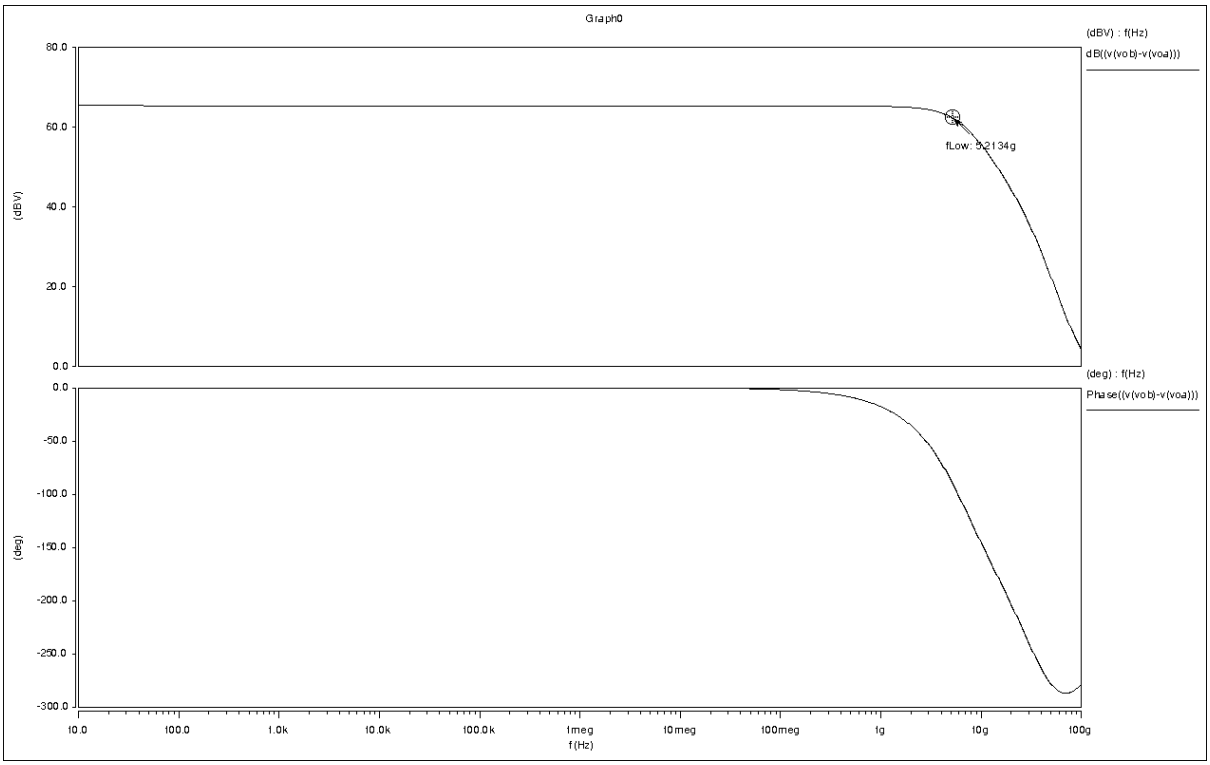
NOTE: Since, in our system we have a third pole at 52GHz, it is expected that the C_f obtained by the above formula will be slightly off. The phantom zero for the circuit is expected to be at $\boldsymbol{Z_f}$**= -4.33GHz.**

The root locus plot with the phantom zero included is shown below:



j) Closed Loop Response Using Phantom Zero Compensation

New Bandwidth, $\omega_{3dbnew} = 5.213\ Ghz$
Gain, $A_O = 65.6\ db$

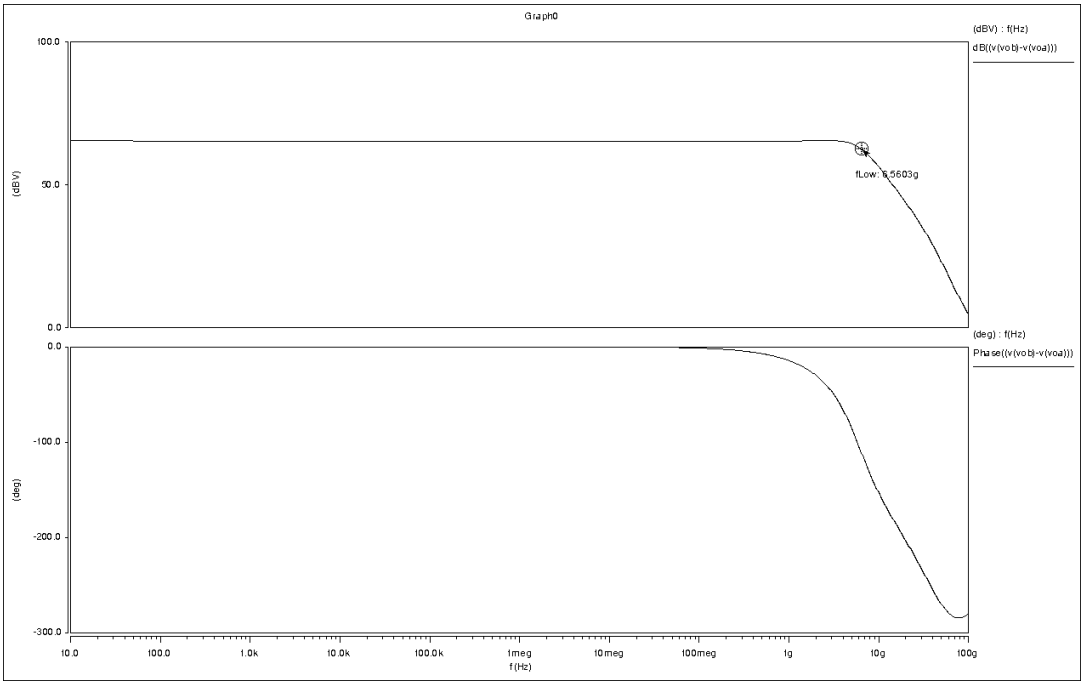


Observation: Clearly, introduction of phantom zero by introducing C_f has improved the phase margin of the loop gain, which in turn resulted in the reduction of the peaking of the closed loop response ($\phi M \geq 60^{o}$). As expected, there is over compensation in this plot as our hand calculated C_f value is a bit higher. Changing the values, we found C_f =25fF to give the highest bandwidth without peaking.
The **New Bandwidth, $\omega_{3dbnew} = 5.213\ Ghz$**

Optimisation: Since, the C_f expected from the formula results in over compensation, as it does not take into account the third non-dominant pole. The value of C_f has been varied a bit around the value obtained by the formulae to obtained the highest bandwidth without resulting in the peaking. Optimised value of C_f obtained is, $C_f \approx 25\ fF$.

Bode Plot for Closed Loop System with Optimised Phantom Zero

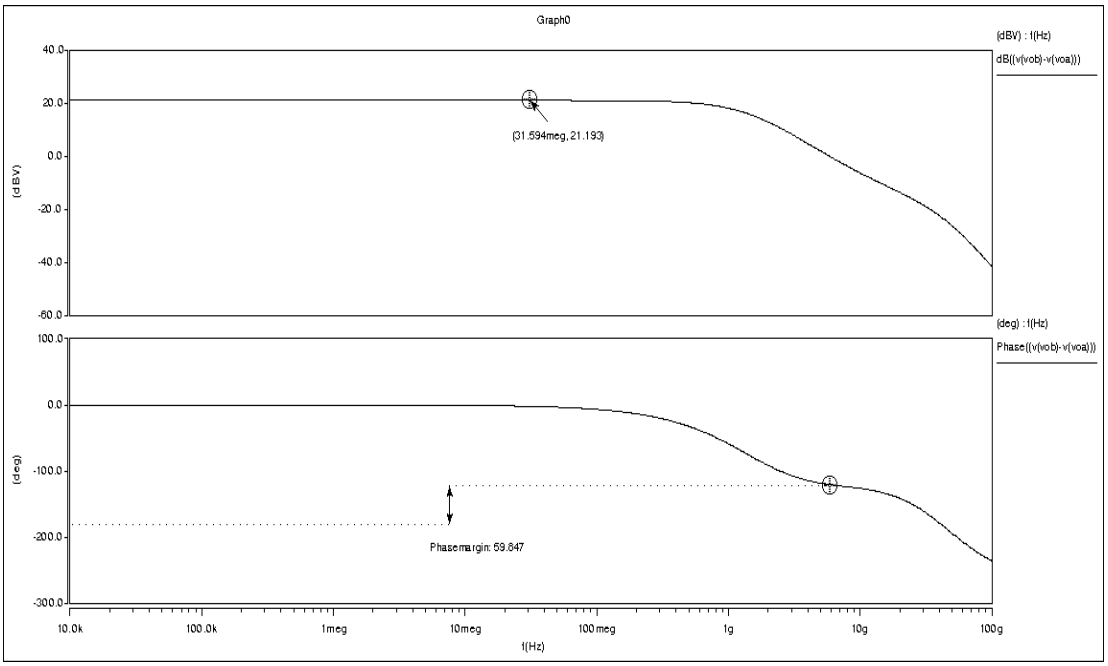
Optimum Bandwidth, $\omega_{3dbnew} = 6.56\ Ghz$
Gain, $A_O = 65.6\ db$



Open Loop Analysis with Optimum Phantom Zero Compensation

After putting C_f in the appropriate places, we get the following open loop bode plots. The phase margin was found to be 59.847 which is ~ 60° hence there will not be any peaking in the system.

Phase Margin, **ϕM = 60°**



k) Input Referred Current Noise Analysis

To determine the input referred current noise of the closed loop system, the input referred noise for the open loop system has been determined and then total input referred for closed system has been determined using the relation (mentioned below) as derived in the notes:

$$\overline{v_i^2} = \overline{v_{io}^2}$$

$$\overline{i_i^2} = \overline{i_{i0}^2} + \frac{\overline{v_{io}^2}}{R_f^2} + 4kT\frac{1}{R_f}\Delta f$$

Where, $\overline{v_i^2}$ - Input referred voltage noise for Closed Loop System
$\overline{i_i^2}$ - Input referred current noise for Closed Loop System
$\overline{v_{io}^2}$ - Input referred voltage noise for Open Loop System
$\overline{i_{i0}^2}$ - Input referred current noise for Open Loop System

1.8.1 Input Referred Noise Calculations for individual stage

Last Stage (Common Collector)

Input referred voltage noise PSD, $\frac{\overline{v_{i1}^2}}{\Delta f} = 4kT(R_L + \frac{1}{2g_m})$

Input referred current noise PSD, $\frac{\overline{i_{i1}^2}}{\Delta f} = 2q(I_B + \frac{I_C}{\beta^2})$

2nd Stage (Differential Amplifier)

Input referred voltage noise PSD, $\frac{\overline{i_{i2}^2}}{\Delta f} = \frac{\overline{i_{b2}^2}}{\Delta f} + \frac{1}{\beta^2}\left(1 + \frac{r_\pi^2}{r_{02}}\right)\frac{\overline{i_{i1}^2}}{\Delta f} + \frac{1}{\beta^2}\frac{\overline{i_{c2}^2}}{\Delta f} + \frac{1}{\beta^2}\frac{1}{r_{02}^2}\frac{\overline{v_{i1}^2}}{\Delta f}$

Input referred current noise PSD, $\frac{\overline{v_{i2}^2}}{\Delta f} = \frac{1}{g_{m2}^2}\left(\frac{\overline{i_{i1}^2}}{\Delta f}\left(1 + \frac{r_\pi^2}{r_{02}}\right) + \frac{1}{r_{02}^2}\frac{\overline{v_{i1}^2}}{\Delta f} + \overline{i_c^2}\right)$

1st Stage (Transimpedance Gain Stage)

$$x = \frac{r_\pi(1 + g_m r_0)}{(r_0 + R_x + r_\pi(1 + g_m r_0))}$$

Input referred current noise PSD, $\frac{\overline{i_{i0}^2}}{\Delta f} = \frac{1}{x^2}\left(\beta^2\frac{\overline{i_{b3}^2}}{\Delta f} + \frac{\overline{i_{c3}^2}}{\Delta f} + \frac{R_x}{R_x + r_\pi}^2\frac{\overline{i_{i2}^2}}{\Delta f}\left(1 + \frac{r_\pi^2}{R_x}\right) + \frac{1}{R_x^2}\frac{\overline{v_{i2}^2}}{\Delta f}\right)$

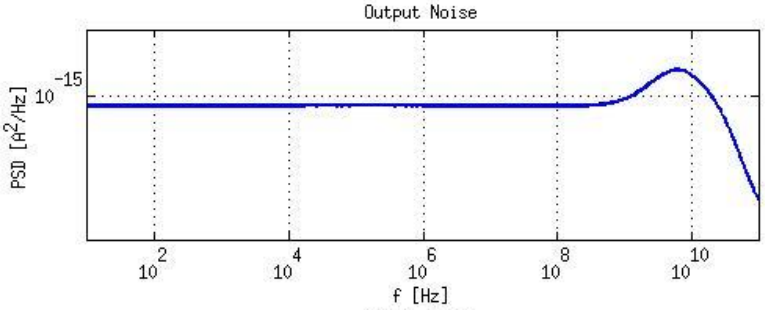
$$y = \frac{r_o}{R_x}\left(\frac{1}{r_o} + \frac{1}{r_\pi} + g_m\right)$$

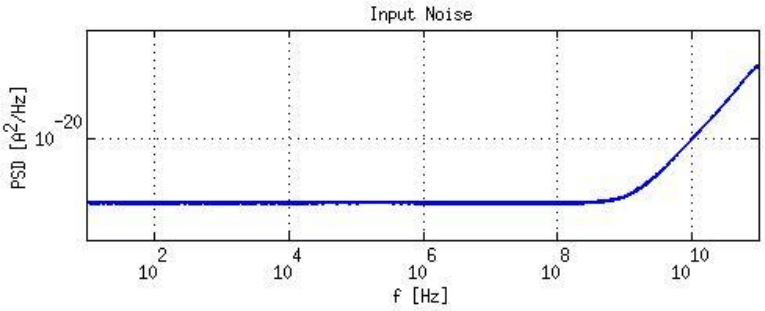
Input referred voltage noise PSD, $\frac{\overline{v_{i0}^2}}{\Delta f} = \frac{1}{y^2}\left(\frac{\overline{i_{i2}^2}}{\Delta f} + \frac{\overline{v_{i2}^2}}{\Delta f}\left(\frac{1}{r_o} + \frac{1}{R_x}\right)^2 + \frac{\overline{i_{b3}^2}}{\Delta f}\left(\beta + \frac{r_\pi}{r_o} + \frac{r_o}{R_x}\right)^2 + \frac{\overline{i_{c3}^2}}{\Delta f}\left(1 + \frac{r_o}{R_x}\right)^2\right)$

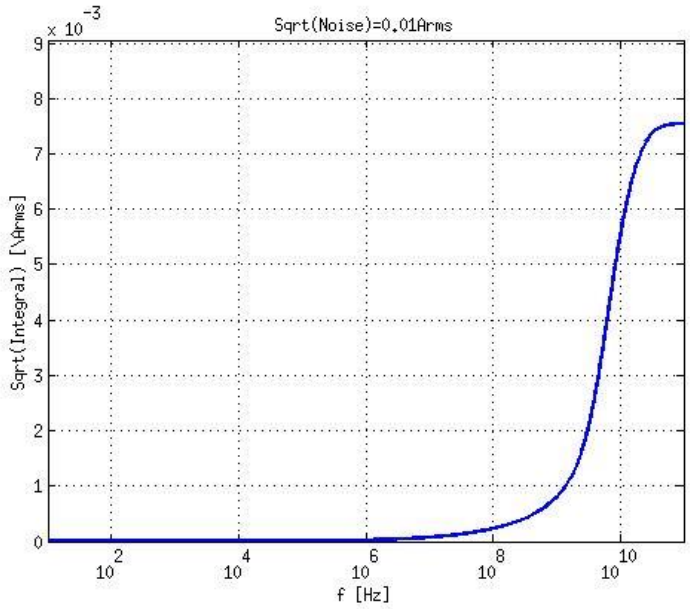
Putting all the values of the variables (given below) in the equations above, we get:

$r_o = 180\ k\Omega, r_\pi = 15\ k\Omega, g_m = 0.02\ \Omega^{-1}, \beta = 300, R_x = 1\ k\Omega, I_c = 0.5\ mA$

i) Spice noise plots are as follows:







DESIGN PROJECT PART 2

This part of the report has been divided into the following subparts:

1) Given Constraints and Selection of a topology
2) Designing to meet all specifications
3) Results
4) Further improvements

1.1 Given Constraints and Selection of a suitable topology

Designing for the same specifications using a MOS device is challenging mainly because of the low transconductance value of MOS devices compared to BJT for the same current. Also, since the given circuit is an optical receiver, its input capacitances are quite high (2pf) which introduce low lying poles and limit the bandwidth that can be extracted from this circuit.

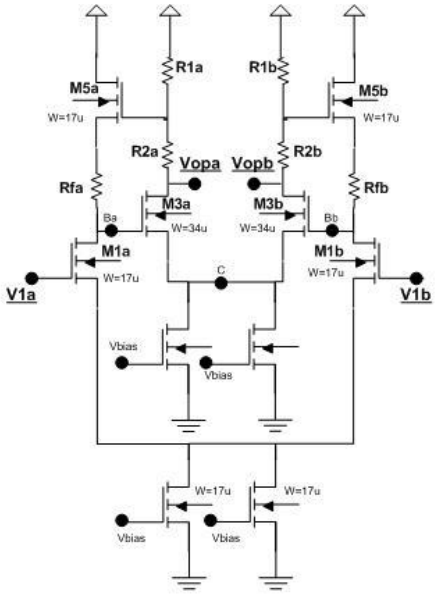
As a first step, we considered converting the given design directly to all MOS. This design is not expected to give us the required gain as MOS devices have lower gm. We selected gm/Id as 10 since we know this is a value at which for the given 0.18um technology, we have a good compromise between high enough transit frequency and low overhead voltage.

We had to change the given resistor values in order to bias the circuit properly. Hand calculating the gain of this circuit, we found the open loop transimpedance much below 28.47 KOhms as was found for the BJT. Then we tried pumping more current into the circuit to increase its gain. After increasing the power to its maximum limit, we were able to achieve the given open loop gain but found that the maximum bandwidth to be extracted from this design was around 1GHz only. Hence we ran into the basic gain bandwidth tradeoff in this design and decided to change the topology.

Considering the problem of achieving required loop gain, we reasoned that extracting gain from a single stage means we need to pump up the current in that stage which leads to higher gm and parasitic capacitances, thus introducing dominant poles, finally leading to a reduced signal bandwidth. Also we would have significant low voltage headroom and high thermal noise problems. Thus we concluded that **cascaded amplifier stages** would be needed. That would enable us to meet the transimpedance requirement without sacrificing on signal bandwidth.

To reduce the loading between adjacent stages, we also decided to use the technique of **alternating local series and shunt feedback** circuits as learnt in class.

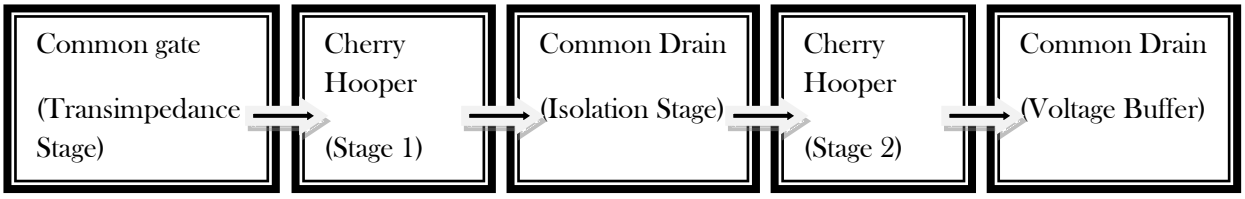
All these considerations brought us finally to use the **Cherry Hooper amplifier** design. After a literature survey on its possible variations, we selected one of the topologies. Shown below is a schematic of the same: [Ref [1],[2],[3]].



NOTE: Body of all NMOS Transistors in the design is connected to Ground (Gnd).
Length of each Transistor = 0.18u
Only M5a,b has body source connected.

This topology is novel in introducing a resistance R2 which helps in increasing gain without compromising on bandwidth.
The active feedback using transistors instead of only transistors helps in introducing positive feedback which increases gain at high frequencies thus increasing the bandwidth of the signal. We also employed global feedback in this circuit so as to get BW(1+To) effect. Since we had to pick some value for Rf we started with 1K and this is a value which will be decided by the gain extracted from our circuit.

We realized that we can break this design problem into three distinct parts – **a common gate stage, a gain stage, voltage buffer stage.** This is a good basic design block diagram as the common gate topology converts the input current signal into a voltage signal while giving moderate gain too. Also, the source follower stage at the end provides low output impedance and helps to prevent loading of this circuit due to output resistances. This is the basic topology followed for the BJT circuit too. Thus our main job should be to design a better gain stage. Following is a basic block diagram of our design and described in the pages ahead is our thought process while designing these individual stages:



1.2 DESIGNING TO MEET ALL SPECIFICATIONS

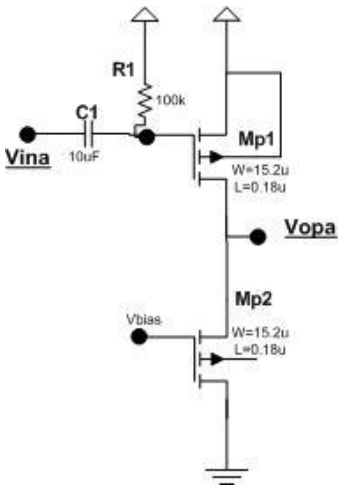
1.2.1 DESIGNING THE COMMON GATE STAGE:

This is the main Transimpedance amplifying (TIA) stage for the circuit. Its TIA gain must be large enough to overcome the noise of the subsequent stage. Since the gain of this stage trades with bandwidth and voltage headroom, the two stages

(TIA and voltage amplifier) need to be designed together so as to optimize the overall performance. Since we have a low supply voltage and we need to maximize bandwidth, the gain of our CG gets limited, thus making the design of the following stage quite difficult. A starting point is to note that the dominant pole of this circuit is introduced at around 1.33GHz by the huge input caps at the Common Base Stage and our effort should be to maintain this as the dominant pole for the MOS as well. We can compromise on the gain of this stage if it leads to a higher dominant pole. The pole at this stage is given by ~ g_m/C_{pa} with g_m=19.23e-3. Thus taking g_m/I_d = 10, the current required would be 2mA to ensure the dominant pole lies at 1.33Ghz as before. We really can't say anything about the drain resistor value at this point.

1.2.2 Middle Stage Buffer Design

We need to have a buffer stage in the middle of the 2 Cherry Hooper stages so as to isolate them and prevent interaction between them which might lead to instability. This is not possible to do using a traditional NMOS buffer as it imposes strict conditions on the input voltage. This is because the input to a Cherry Hooper stage requires at least (2*Vov + Vth) to keep the transistors in saturation. It comes to about 0.9 V. The output of this buffer will be the input of the next CH stage. Thus we need at least 0.9V output from the buffer. This means its input voltage should be at least (0.9+ Vov + Vth) = 0.9 + 0.2+ 0.5= 1.6V. Thus we are left with very little headroom. A similar problem occurs when using PMOS buffers also, hence we decided to go for a different topology using *capacitive coupling*. A schematic of the design looks as follows [Ref (Razavi book)]:



The capacitance used in this design is kept high at 10uF so that it becomes a short for AC analysis and does not affect our frequencies of interest. Also, it does away with the overhead problem by breaking the circuit at DC voltages. Base resistance is kept large enough to isolate the signal path from the low impedance introduced by the transistor.

1.2.3 Designing the common drain (source follower end stage)

The last stage would be a source follower stage with attenuation as low as possible. But since we have power restrictions we decided to restrict its current to 0.1mA and got an attenuation of 0.7 from it.

1.2.4 Designing the Cherry Hooper Stages

Finally, we came to designing the cherry hooper for maximum gain while keeping the poles introduced by it as large and as far apart as possible.

Since we also have a power and noise limitation to consider, we figured it would be good to go with only two cherry hooper stages. While deciding the resistor values (R1, R2, Rf) for each cherry hooper, we found that it is not easy to hand calculate their optimum values because of the following considerations:

1) Proper voltage biasing to ensure all transistors work in saturation mode – This becomes a big consideration as it is very difficult to do a back of the envelope calculation for resistances because :
   The supply voltage is limited to 1.8V
   Devices are in stack which worsens the overhead problems
2) Try to keep the poles introduced by it as large as possible and as far apart from each other as possible. Widely spaced poles lead to a better root locus plot, allowing us to extract gain without making the system unstable.
3) Extract at least the minimum amount of gain
4) Limited availability of power

Hence we decided to write a Matlab code for the same, which took into account all the above conditions while iterating over a range of possible values. We determined the range of these values by hand and then used the Matlab code for finding the exact combination. [Code attached in the appendix]

We noted that values of C_{gs} and C_{ds} change with the amount of current flowing through them hence these were not taken as fixed values but calculated dynamically by the script. Also, the miller capacitances change as a function of gain which again depends on the current flowing through the transistors. Hence, each stage's gain was also computed by the script for every iteration.

We need to extract a certain amount of gain from this circuit. This minimum gain to be extracted from the cherry hooper was found using:

The gain of the circuit = a_o= A(CG) * A(cherry) * A(Isolation Buffer) * A (cherry) * A (CD) = 11471 (Spice result)

From the previous designing,

A(CG)= $\frac{1}{g_{mb}+\frac{1}{R_{fb}}}\,(g_{mb}R_{1a})$ ~ arnd 400 in BJT

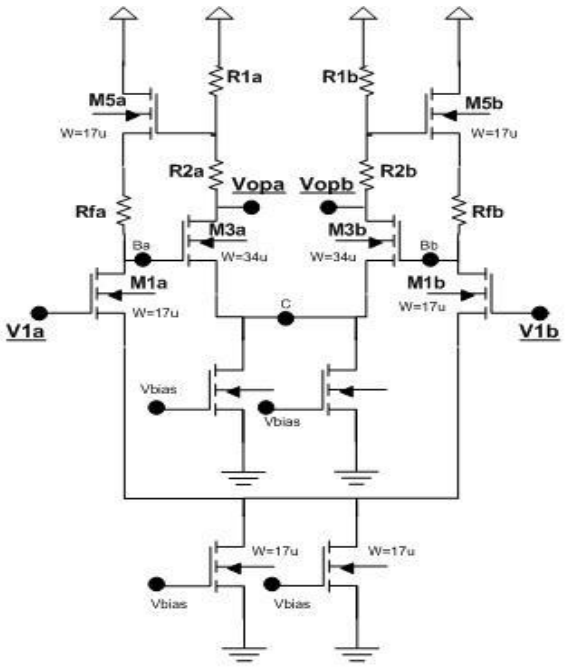
A(Cherry)= $\frac{V_{out}}{V_{in}} = \frac{g_{m1}(R_1+R_2)(\frac{1}{g_{m5}}+R_f)}{2(\frac{1}{g_{m3}}+R_1)}$

A(Isolation Buffer)= $\frac{R_o}{\frac{1}{g_{m3}}+R_o}$ = 35/36= 0.9

A(CD)= $\frac{R_L||R_f}{\frac{1}{g_{m3}}+R_L||R_f}$ = 0.7

These rough calculations enable us to set a minima on the gain of the cherry hoop stage and ensure during every iteration that we are above this value.
Finally, since we also have a constraint on power and since we are using two stages, we decided to set a limit on the total current flowing in the Cherry Hooper to 2mA.

After all these conditions were imposed we got several combinations of resistances and currents which were meeting all of the conditions. But we finally selected a design which seemed to attain the maximum bandwidth with the least current. Our final Cherry Hooper looks like this:



NOTE: Body of all NMOS Transistors in the design is connected to Ground (Gnd).
Length of each Transistor = 0.18u
Only M5a,b has body source connected.

And the Matlab generated optimized values are:
R1= 10
R2= 635
Rf= 125
I1= 0.5mA,w1= 17u
I2= 0.9mA, w3= 30.68u
Ix= 2.3mA
Wx=78.4u
Rx= 400 Ohms

1.3 RESULTS

1.3.1 HAND AND SPICE CALCULATIONS COMPARISON

The design values obtained from the Matlab script were as follows:

3.1.1 Bias point voltages

Nodes	HAND	Spice	%Error	Nodes	HAND	Spice	%Error
V1a	1	1.0773	-7.18	Vina	1.3	1.32	-1.51
V1a_	1	0.927	7.87	Vinb	1.3	1.32	-1.51
V1b	1	1.0773	-7.17	Voa	0.5	0.533	-6.19
V1b_	1	0.927	7.87	Vob	0.5	0.533	-6.19
VB	0.7	0.676	3.55	Vopa	1.3	1.32	-1.51
Vba	0.9	0.88	2.27	Vopa_	1.3	1.32	-1.51
Vba_	0.9	0.888	1.35	Vopb	1.3	1.32	-1.51
Vbb	0.9	0.88	2.27	Vopb_	1.3	1.32	-1.51
Vbb_	0.9	0.888	1.35	Vsa	1	0.927	7.87
Vbias	0.9	0.939	-4.15	Vsb	1	0.927	7.87
Vdiff_1	0.2	0.233	-14.4	Vua	1	0.935	6.95
Vdiff_1_	0.2	0.218	-8.26	Vua_	1	0.94	6.38
Vdiff_2	0.2	0.191	4.71	Vub	1	0.935	6.95
Vdiff_2_	0.2	0.197	1.52	Vub_	1	0.94	6.38
Vga	1.8	1.8	0	Vva	1.75	1.79	-2.23
Vgb	1.8	1.8	0	Vva_	1.75	1.79	-2.23
Via	0.2	0.237	-15.61	Vvb	1.75	1.79	-2.23
Vib	0.2	0.237	-15.61	Vvb_	1.75	1.79	-2.23

3.1.2 Open loop poles

The following equations were derived to calculate the open loop poles of our design:

$$\tau_b = (20^{-15}\left(1+\frac{1}{Av(CherryHooperPart1)}\right) + 20^{-15}(1+Av(CherryHooperPart2) + 50^{-15})(R_f + \frac{1}{gm_5})$$

$$\tau_c = (Cgd_3\left(1+\frac{1}{Av(CherryHooperPart2)}\right) + Cgs_1 + Cgd_1\big(1+Av(CherryHooperPart1)\big)(R_1 + R_2)$$

$$\tau_a = (Cgd_x + Cgs_1 + Cgd_1\big(1+Av(CherryHooperPart1)\big)R_x$$

From these formulas we found the open loop poles to be at (-1.33g, - 2.24, -4.61 and -5.82) GHz.
Spice results: -1.36 GHz, -2.2772GHz, -2.6559 GHz,-9.47GHz

3.1.3 Open loop gain

The overall gain of the system can be calculated as = A(CG)* Acherry hooper * AcherryHooper* A (Buffer)* A(CD) . Now,

A(CG)= $\frac{1}{g_{mb}+\frac{1}{R_{fb}}}\,(g_{mb}R_{1a})$ = 383.33

g_{mb}=23e-3

The gain for a cherry hooper stage is given by [Ref [2]]:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}(R_1 + R_2)(\frac{1}{g_{m5}} + R_f)}{2(\frac{1}{g_{m3}} + R_1)}$$

Here,

g_{m1}= $10i_1$= 5e-3

g_{m5} = $10i_1$ = 5e-3

g_{m3}=$10i_3$=9e-3

Ro=35K

∴ A(CherryHooper) = 4.327

A(Buffer)= $\frac{R_o}{\frac{1}{g_{m3}}+R_o}$ = 35/36= 0.9

A(CD)= $\frac{R_L||R_f}{\frac{1}{g_{m3}}+R_L||R_f}$ = 0.7

Plugging in the design values we get gain as = 4521.5 Ohms
Thus open loop gain = 4.521 Ohms
Spice open loop gain= 5.72 Ohms

The difference in these values arises from the fact that we have assumed current as exact values of 1ma, 2ma etc.

3.1.4 Closed loop gain

This is given by the formula

$$TIA = \frac{2a_o}{1 + a_o f}$$

∴ Hand calculations = 1637.93
Spice = 1702.5

3.1.5 Phase margin

Spice result = 181.57°

3.1.6 Closed loop poles

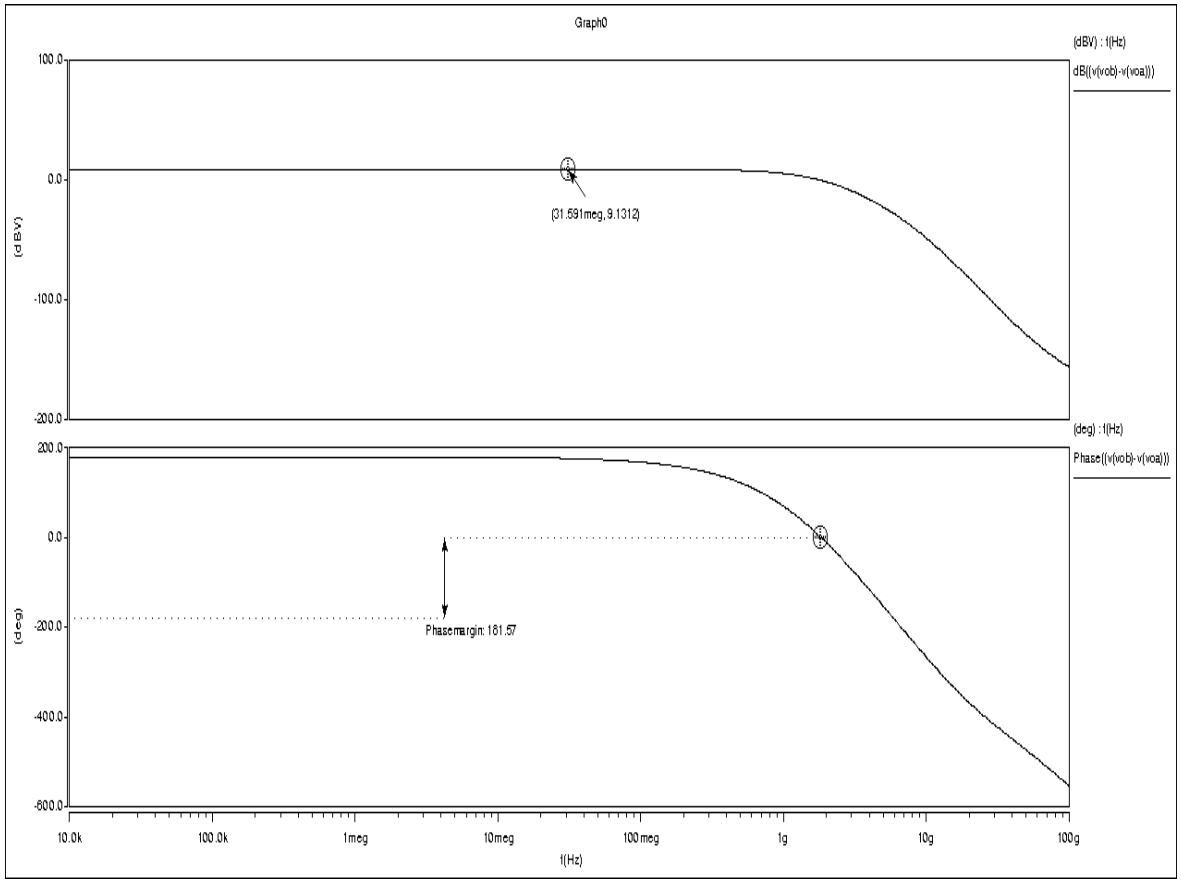
Spice results = (+ 0.387 ± j2.08)g , (-11.17 ± j4.32)g, -68.077g

3.1.7 Bandwidth

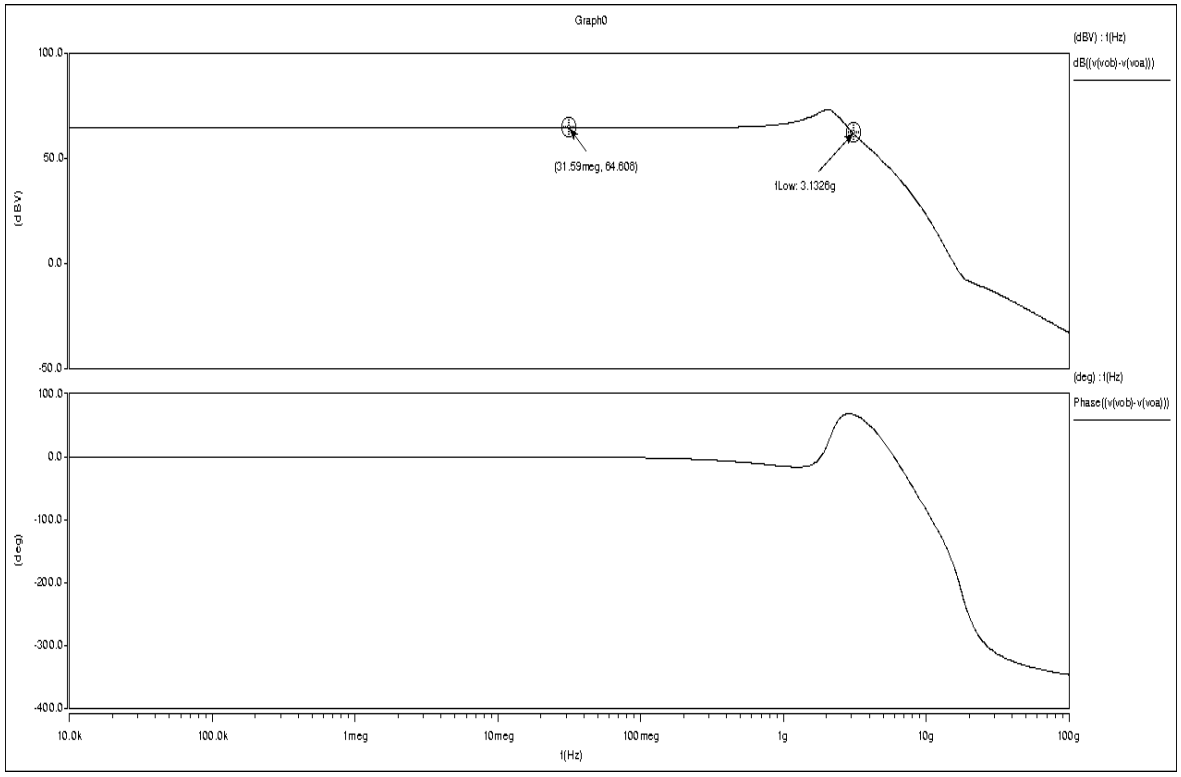
Spice BW = 3.13GHz

Following are bode and root locus plots for this design for open and closed loops respectively:

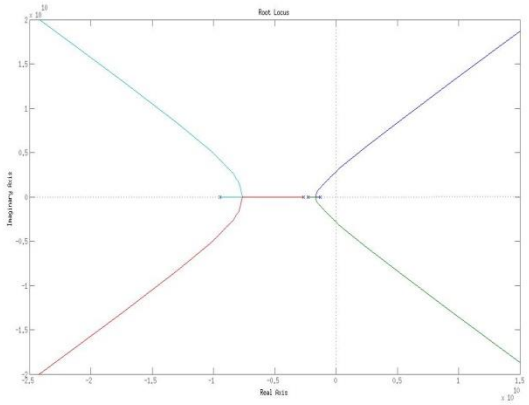
Open loop plot:



Closed loop Plot:



We see the presence of a positive open loop pole in the response of this system from both the .pz analysis and the phase margin plot. To gain further insight on the origin of this positive pole, we plotted a root locus plot of this system and observed the point at which gain was T_o.



This point was lying in the right half plane and hence our conclusion was to reduce T_o value to get closed loop poles in the LHP. For this the only knob that we have at this point is R_f. Increasing R_f would reduce T_o but reduce our circuits's bandwidth also. Again from the root locus plot we found the values of To at which the system was stable and found a range of R_f values. A value of R_f=2K was chosen as it brought T_o well into the stable region.

<u>Capacitive Feedback (Phantom Zero) Compensation</u>

The observed phase margin is negative which should improve now by increasing the Rf value. To improve the ϕM even more, phantom zero technique has been utilized to introduce a zero at left half plane so as to increase the stability of the design. Capacitance C_f has been added in the global feedback of the design as shunt feedback to introduce zero and to improve phase margin. To calculate this Cf value we can use the following formula.

$$T_o = \frac{2\|Z_f\|^2}{\|p_2\|\|p_1\|}$$

$$\text{Where } Z_f = \frac{1}{2\pi R_f C_f}$$

p_1= - 1.33 Ghz
p_2 =- 2.24 Ghz
T_o= 4.521
R_f=2K

However, looking at the system's open loop poles, we can conclude that the above formula is really not valid here as p3 >>p1 and p2 is not satisfied here. The better way should be to make a root locus plot and observe the 45 point.
Thus C_f = 30.68fF
Simulated C_f value from Spice was found to be 50fF which indicates that this is really not an accurate method.

We plugged in this value of R_f and C_f in our spice file and the new closed loop poles observed were all in the LHP plane.

Thus, *after making the above changes* our final design gives:

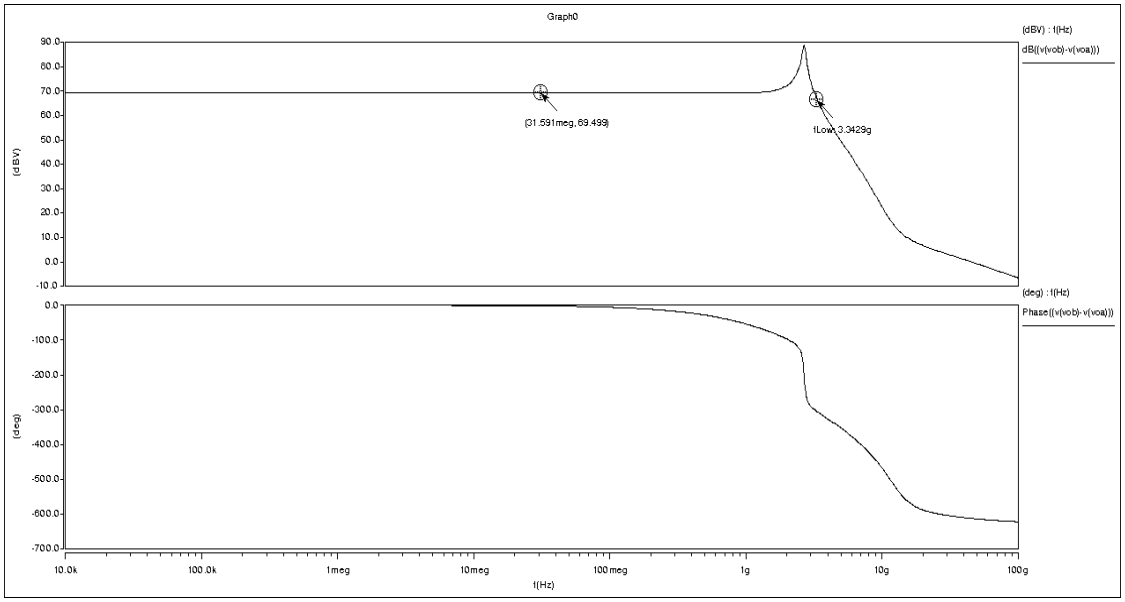
Closed loop gain = 2985 Ohms
Closed loop poles= -1.5GHz, (-6.44 ± j6.05) GHz, (-13.175± j5.395)GHz

Bandwidth = 3.34GHz

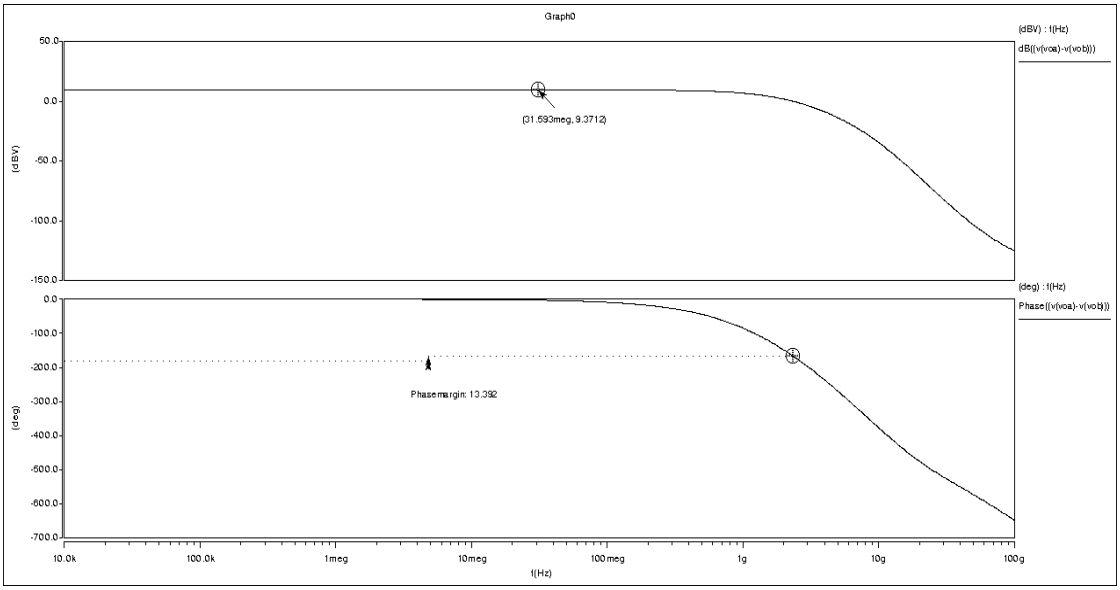
Open loop gain = 9.3972 db = 2.95
Open loop poles = -1.344GHz, -2.297GHz, -2.647GHz, $(-4.71 \pm j22.44)GHz$

Phase margin = 13.392 Degrees
Power consumption =24.4mW

Closed loop Bode Plot



Open Loop Bode Plot



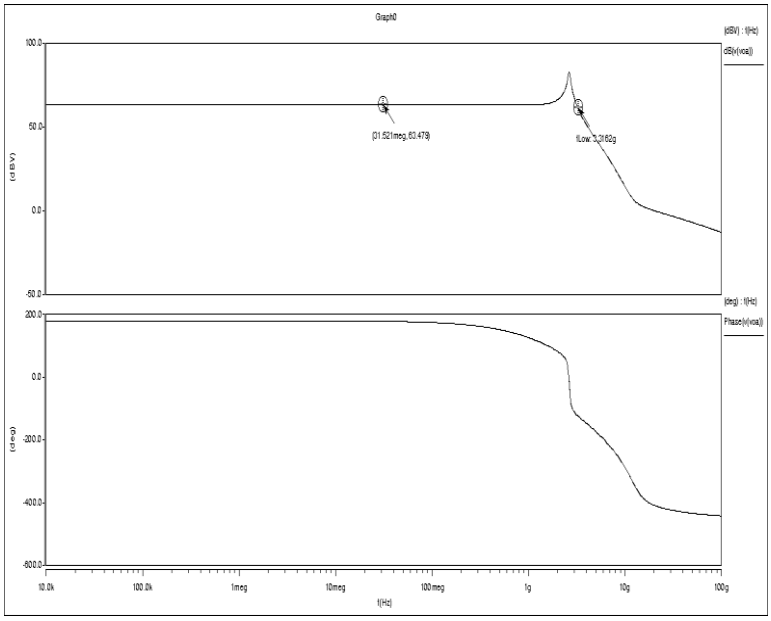
This design has low input referred current noise as well as found from a .noise analysis on Spice. It has noise on the order of nA^2/Hz and is comparable to that found from the BJT design. MOSFETs are inherently less noisy than Bipolar as they do not create noise when in cutoff region. (PSD plot for design in Appendix)

4.0 FURTHER IMPROVEMENTS

4.1 Miller Effect Neutralization

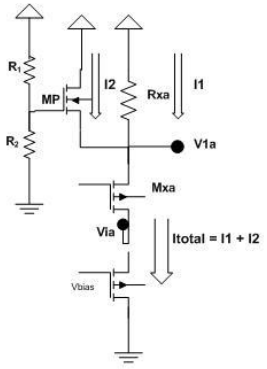
In the two gain stages of cherry hooper configuration, the C_{gd} capacitance increases due to miller effect and results in lowering of the other non-dominant poles, which results in lowering the phase margin of T_o and also, the bandwidth. Miller effect can be reduced using the neutralization techniques in differential gain stages by connecting external capacitance, $C_{neutral1,2} \approx C_{gd1,3}$ to the reverse polarity output terminal, so as to cancel the miller effect ($C_{eff} = C_{gd1}(1 + A_v) + C_{neutral1}(1 - A_v) \approx 2C_{gd1}$). This technique has been utilised to reduce the miller effect and to increasing the non-dominant pole of open system, however as the effect tries to move the pole at 'A' to higher frequency, it results in interaction of the pole at 'A' with the pole at 'C', 2nd stage of cherry hooper configuration. Hence, it could not be utilised to large improvement in bandwidth.

Observation: It can be observed that the neutralization technique and the pole splitting technique are complementary to each other. The extend of the pole splitting and neutralization implementation is comparatively very small and limited due to the close proximity of the 2 non-dominant poles of the cherry hooper stage (poles at: 'A', 'B'). As a result, balance have to be maintained since, phase margin can not be extend to large improvement by just these two techniques.



4.2 Gm Enhancement

Since, C_{pa} (=2pF) is very large as compared to intrinsic capacitances the dominant pole in the open loop system is determined by the transimpedance stage $C_{pa.}$ As a result, the equivalent resistance seen by the node at Input (i.e. $R_{eq} = \frac{1}{g_m}$) have to be minimised. Hence, the current through the transimpedance gain stage have been increased to increase gm. To maintain the operating point biasing through the stage pmos in parallel to the resistance (Rx) have been added as shown in the figure below.



NOTE: R1 & R2 values have been determined to bias PMOS transistor, to provide required current.

4.3 Pole Splitting

To increase the phase margin of the T_o, pole splitting has been introduced using the $C_f{}'$ capacitors in the local feedback of each cherry hooper stage in parallel to $R_f{}'$ to introduce higher miller capacitance, so as to move the pole at 'A' to a lower frequency and the pole at 'B' to a higher frequency.

However, the point of concern in the design is that as the pole splitting is introduced in the local feedback loop, it results in bring the pole at 'A' closer to the dominant pole (at Input – C_{pa}). Hence, higher pole splitting results in phase margin degradation due to the interaction with dominant pole and cannot be increased further to increase the phase margin, which results on limiting the extend of pole splitting possible apart from bandwidth reduction.

4.4 Local Capacitive feedback

Capacitance, C_f' in parallel to R_f' in local cherry hooper stage could be added using the shunt feedback similar to the phantom zero concept to minimize peaking in the closed loop response and to increase the phase margin of the open loop system.

APPENDIX

REFERENCES

1) 10 Gb/s CMOS Limiting Amplifier for Optical links - Rui Tao, Manfred Berroth

2) Modified CMOS Cherry-Hooper Amplifiers with Source Follower Feedback in 0.35 μm Technology - Chris D. Holdenried, Michael W. Lynch, James W. Haslett

3) 6-k 43-Gb/s Differential Transimpedance-Limiting Amplifier With Auto-Zero Feedback and High Dynamic Range - Hai Tran*, Member, IEEE*, Florin Pera*, Member, IEEE*, Douglas

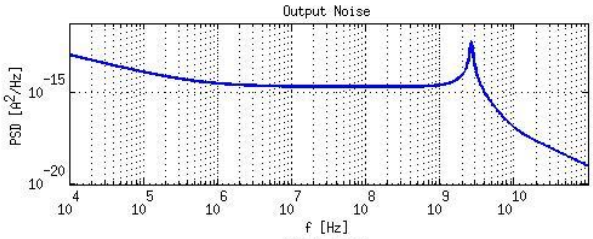
4) Bandwidth enhancement techniques for transimpedance Amplifier in CMOS Technologies – Chao Hsin Lu and Wei – Zen Chen

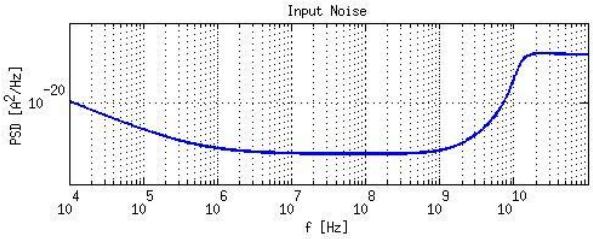
5) Design of Analog CMOS Integrated Circuits – Razavi

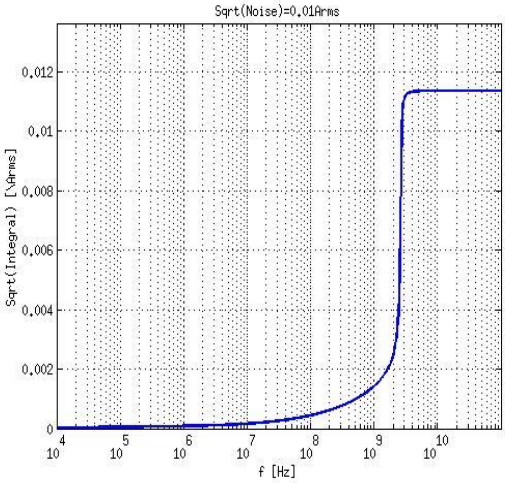
6) A 15 GHz, 1.8V, Variable-Gain, Modified Cherry-Hooper Amplifier - Justin Abbott, Calvin Plett, and John W. M. Rogers

NOISE PLOTS:

The following noise plots were obtained from Spice for our MOS final design:







Matlab optimization code

```
%%% variables r1 gm3 gm5 Rf_ r2
clc
clear all
%To=17.3181;
Cpa=2e-12;
Cgs1=30.0e-15;
Cgd1=10.0e-15;
Cgs3=64.59e-15;
Cgd3=21.39e-15;
Cgsx=98.7e-15;
Cgdx=32.8e-15;
Cgsy=15e-15;
Cgdy=5e-15;
Cgsm=22.4e-15;
Cgdm=7.3e-15;
Rl=250;
gdsm=138.9771e-6;
gmm=4.64e-3;
Rx=400;
gmx=18.11e-3;
gmy=3.3e-3;
gm5=5.6e-3;
gm3=11.75e-3;
r1=10;
```

```
r2=700;
Rf=90;
Rb=10e3;
Av_cherry_part1=gm5*(Rf+1/gm5);
Av_cherry_part2=gm3*(r1+r2);

 tb=(Cgd1*(1+1/Av_cherry_part1)+Cgd3*(1+Av_cherry_part2)+Cgs3)*(Rf+1/gm5);
 ta=(Cgdx+Cgs1+Cgd1*(1+Av_cherry_part1))*Rx;
 tc=(Cgd3*(1+1/Av_cherry_part2)+Cgsm/(1+gmm/gdsm)+Cgdm)*(r1+r2);
 ta_=(Cgs1+Cgd1*(1+Av_cherry_part1))*1/gmm;
 tb_=tb;
 tc_=(Cgd3*(1+1/Av_cherry_part2)+Cgsy/(1+gmy*200)+Cgdy)*(r1+r2);
  pa=1/ta/2/pi
  pb=1/tb/2/pi
  pc=1/tc/2/pi
  pa_=1/ta_/2/pi
  pb_=pb
  pc_=1/tc_/2/pi
  tdominant=(Cgsx+Cpa+2*Cgdx)*1/gmx;
  pdominant=1/tdominant/2/pi
 %ta=(Cgd3*(1+1/Av_cherry_part2)+Cgsy/(1+gmy*Rl) + Cgdy)*(r1+r2);

Avmin=1.2e4;taubmin=10000;tauAmin=1000;
for ix=0.1e-3:0.2e-3:2.5e-3
    ix
    for Rx=100:50:2000
        Va=ix*Rx;
        if (Va>=0.9 && Va<=1.6)
            for r1=10:20:100
                for r2=10:25:700
                    for i2=0.1e-3:0.2e-3:2.5e-3
                        for i1=0.1e-3:0.2e-3:2.5e-3
                            for Rf=10:25:500
                                gm3=10*i2;
                                gm5=10*i1;
                                gmx=10*ix;
                                Av_cherry_part1=gm5*(Rf+1/gm5);
                                Av_cherry_part2=gm3*(r1+r2);
                                Cgsx=100e-15*ix/2e-3;
                                Cgs1=100e-15*i1/2e-3;
                                Cgs3=100e-15*i2/2e-3;
                                Cgd3=0.24*Cgs3;
                                Cgd1=0.24*Cgs1;
                                Cgdx=0.24*Cgsx;

                                if ((Va<1.7-i2*r1-i1*Rf) && (i2*r2-
i1*Rf<1.5) && (i2*(r1+r2)<=1.45) && (i1*Rf+i2*r1<0.1)...
                                        && (Va+i2*(r1+r2)>=1) &&
(i1+i2<2.5e-3))
                                    %4353453
                                    Av_ch=(r1+r2)*(1+gm5*Rf)/(1/gm3 + r1);

Avtot=0.5*(Av_ch^2)*Rx*gmx*Rf/(1+gmx*Rf);

                                    if (Avtot>Avmin)
                                        taub=(20e-
15*(1+1/Av_cherry_part1)+20e-15*(1+Av_cherry_part2)+50e-15)*(Rf+1/gm5);
                                        tauC=(Cgd3*(1+1/Av_cherry_part2)+
Cgs1+Cgd1*(1+Av_cherry_part1))*(r1+r2);

tauA=(Cgdx+Cgs1+Cgd1*(1+Av_cherry_part1))*Rx;
```

```
                                        tau_dominant=(Cgsx+Cpa+2*Cgdx)/gmx;

%ta=(Cgd3*(1+1/Av_cherry_part2)+Cgsy/(1+gmy*Rl) + Cgdy)*(r1+r2);
                                        if((tau_dominant< 1.5e-10) &&
(taub<10e-11) && (tauA<3e-11) && (tauC<10e-11))
                                            %dfd
                                            if
((taub<taubmin)||(tauA<tauAmin)&&(abs(taub-tauA)>0.001e-9))
                                                taubmin=taub;
                                                tauAmin=tauA;
                                                tauCmin=tauC;
                                                r1best=r1;
                                                r2best=r2;
                                                i1best=i1;
                                                i2best=i2;
                                                ixbest=ix;
                                                Rxbest=Rx;
                                                Vabest=ix*Rx;
                                                rfbest=Rf;
                                                Avbest=Avtot;
                                                Vabest=Va;
                                                pabest=1/tauAmin/2/pi;
                                                pbbest=1/taubmin/2/pi;
                                                pcbest=1/tauCmin/2/pi;
                                            end
                                        end
                                    end
                                end
                            end
                        end
                    end
                    %%disp('running');
                end
            end
        end
end
addpath ('/usr/class/ee214/matlab');
load techchar.mat;
wx=ixbest/(lookup_idw(tech, 'n', 0.18e-6, 10))
w1=i1best/(lookup_idw(tech, 'n', 0.18e-6, 10))
w2=i2best/(lookup_idw(tech, 'n', 0.18e-6, 10))
```