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EE391 – Independent Study

Comparative Study of Transimpedance Amplifier Design for MEMS Resonators for GSM Communication Systems

Submitted by

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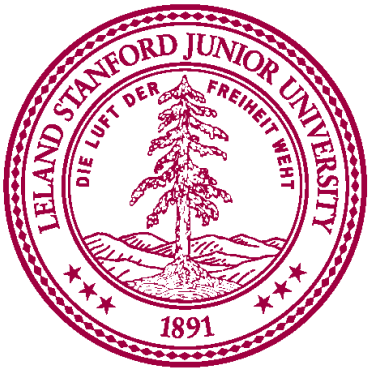
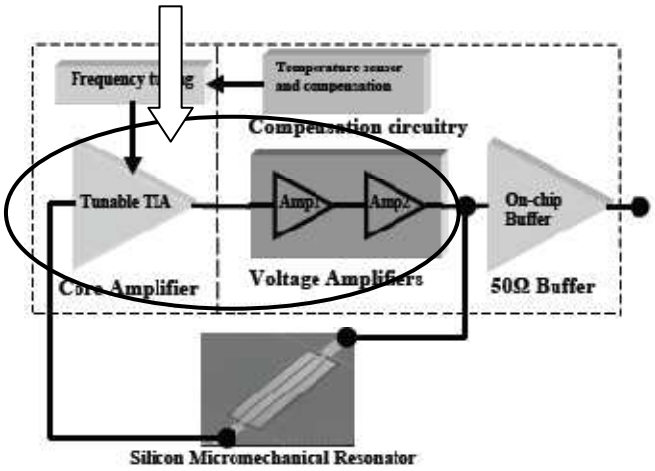


1. Introduction

Modern Transceivers in GSM communication rely on off-chip, bulky low frequency (~100MHz) quartz crystal oscillators. Silicon micromechanical oscillators are suitable alternative to quartz crystal oscillators due to their small form-factor, higher frequency and integration potential with ICs.



In MEMS, electrostatic transduction is a convenient method of electronically sensing the motion of a mechanical resonator. To achieve electrostatic sensing, a bias voltage (V_{BIAS}) is applied in between the moving MEMS device and stationary sense electrode. The motion of MEMS device modulates the capacitance (C_{SENSE}) between the device and the electrode, thereby injecting a signal current (i_{SIG}) into the sense electrode, with $i_{SIG}=V_{BIAS}$ ($\delta C_{SENSE}/\delta t$). A transimpedance amplifier is then used to convert i_{SIG} into a voltage. Often this voltage is applied back to the resonator's input with appropriate gain and phase to generate closed-loop oscillations.

1.1 Motivation. High Q lateral-mode silicon micromechanical resonators are suitable for multi frequency references but exhibit high motional resistance. This motional resistance can be reduced at the expense of larger transduction area and hence larger parasitic capacitance. This high motional resistance combined with the large parasitic capacitance of the resonator restricts the realization of oscillator and development of low-power, high gain Transimpedance Amplifier (TIA) becomes necessary. Unfortunately, in MEMS applications, the amplitude of i_{SIG} is limited to the nano ampere range because of the constraints on the bias voltage, the mechanical displacement of the resonator, or the achievable sense capacitance. As a result, TIA with large gain and small input-referred noise are desirable.

Moreover, low phase noise closed loop oscillator applications like for GSM communication systems require TIA phase response near zero degrees at the frequency of oscillation (f_{osc}), which necessitates a TIA bandwidth well beyond f_{osc}. This phase shift from TIA can be minimized by choosing the amplifier bandwidth to be at least 10X greater than oscillator frequency. Since, the required local oscillator frequency in 2G-GSM technology is ~110MHz, the bandwidth of the TIA is kept around 10x f_{osc} i.e. ~1GHz.

1.2 Specifications. Keeping the constraints and requirements in mind, the specifications targeted for the design of TIA meant for MEMS resonators used in GSM communication are as follow:

1. TIA Gain: 60db - 80db: 1kohm - 10kohm
2. Bandwidth: ~1 GHz
3. Input-referred Noise Current: Minimize

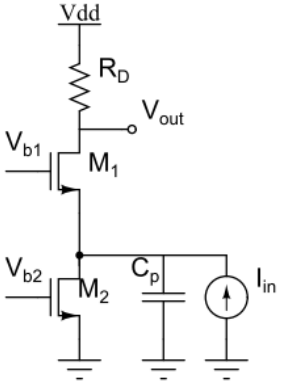
High Speed Transimpedance amplifiers (TIAs) used in MEMS resonators present challenges in the form of tradeoffs between input noise current, speed, transimpedance gain, power dissipation and supply voltage.

1.3 Tradeoff Parameters

- Input Noise Current
- Speed (Bandwidth)
- Gain
- Power Dissipation
- Supply Voltage

2. Design Topologies

2.1 Common Gate Configuration



2.1.1a Gain: Basic topology for designing a Transimpedance amplifier is to have a common gate configuration as shown in figure (on the left). The transimpedance gain of the design is given by, $A_v \approx -R_D$. It clearly indicates that to have higher gain, R_D needs to be increased. However, the maximum value of R_D is limited by the voltage headroom available. As a result, at smaller technologies the topology is limited by the gain and may not be a suitable choice for the given specifications of TIA design.

2.1.1b Bandwidth: The input impedance of the design is, $Z_{in} \approx \frac{1}{g_m}$, hence proper biasing can easily result in low input impedance, which results in dominant pole ($w_p = \frac{1}{g_m C_p}$) at high frequency and hence, high bandwidth (~few 100's MHz). However, increasing value of R_D results in introducing pole ($w_{p2} \approx \frac{1}{C_L R_D}$), where C_L is the load capacitance, may result in lowering down of bandwidth further.

2.1.1c Noise: Noise current of transistor, M_2 and R_D are referred to the input directly. The overall input referred noise current is given by,

$$\overline{i_n{}^2} \approx \frac{4kT}{R_D} + 4kT\gamma g_{m2}$$

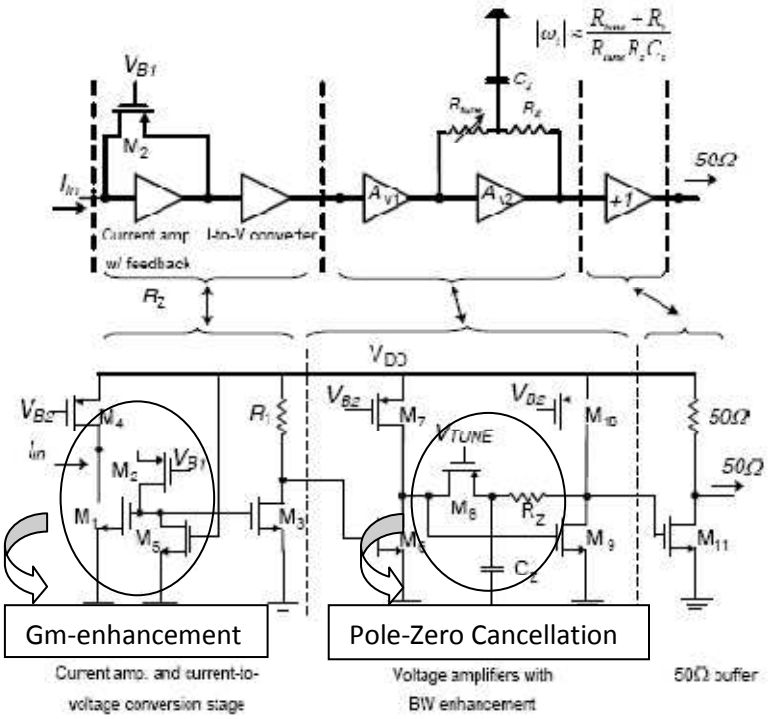
Note: This expression does not include the noise contribution from M_1 since, channel length modulation has been neglected for simplification, which when taken into account results in noise current contribution from M_1 as well.

Remark: The noise expression clearly indicates that to design a low noise transimpedance amplifier large value of R_D is required, which is constrained by the voltage headroom. As a result, common gate configuration may not be suitable for very low noise TIA design as per the required specifications.

2.1.2 Techniques to improve the performance of common-gate configuration

Various topologies being implemented to enhance properties of the common gate configuration are as follow:

1. Gm – enhancement
2. Cascode Topology



Gm-enhancement (Bandwidth Improvement Techniques)

Since, input parasitic capacitance is pretty large, it leads to lower dominant pole on input side and hence, lower bandwidth of the system. To increase, the bandwidth of the design, local feedback can be utilized, so as to reduce input impedance by a gain factor (A) such that, input impedance $Z_{in} \approx \frac{1}{Ag_m}$ where, A is the gain of the opamp.

This helps in moving the dominant pole from $w_p = \frac{1}{g_m C_p}$ to $w_p{}' = \frac{1}{Ag_m C_p}$ resulting in large bandwidth.

Other technique:

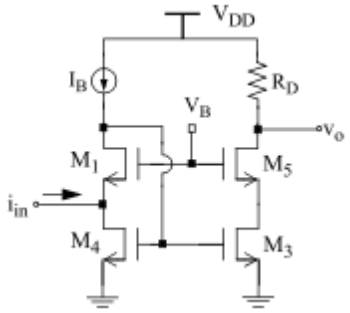
- Pole-Zero Cancellation

$$w_z \cong \frac{R_{tune} + R_z}{R_{tune} R_z C_z}$$

Pole-zero cancellation technique has been implemented [3] by introducing a zero in the feedback path as shown in figure above by utilizing the resistive feedback topology (discussed later in the report) at later stage, so as to cancel the secondary pole introduced by the system and hence, to improve the bandwidth further. It should be noted that the gm-enhancement technique has been used in the 1st stage of the TIA.

2.2 Cascode Topology

The cascade topology has been implemented in TIA design [5]. This technique utilizes the common gate configuration and has high bandwidth.



2.2.1. Characteristics of the topology

- Gm Enhancement
- Wide output swing and low input impedance.
- Broadband but a relatively high input noise current because the noise currents due to R_D and transistors are directly referred to the input.
- To minimize the noise current and achieve high gain due to R_D, dc voltage drop across R_D must be increased, which is limited by the voltage headroom available for the stack of two transistors. As voltage overdrive of transistors decreases it results in higher gm and hence, high drain noise current due to transistors.

- Input impedance is given by,

$$Z_{in} = \frac{1}{g_{m1}(1 + g_{m4} R_B)}$$

R_B is the equivalent resistance of bias current source (I_B).

Properties	Value	Remark
Gain	$A_v \approx -R_D$	
Bandwidth	$w_{bw} = \frac{1}{2\pi g_{m1} g_{m4} R_B}$	
Input Referred Current Noise	$\overline{\iota_n{}^2} \approx \frac{4kT}{R_B} + \frac{4kT}{R_D} + 4kT\frac{2}{3}g_{m3} + 4kT\frac{2}{3}g_{m4} + 4kT\frac{2}{3}g_{m5} + \frac{8kT}{3g_{m3}(z_{in}{}^2)}$	

Remark: The cascade topology suffers from very high input referred noise current and hence, is not suitable for the TIA design for MEMS resonators.

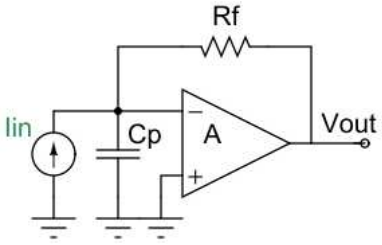
2.2.2 Drawbacks of Common Gate Configuration

- Since, channel length modulation is present in transistors, the drain current noise contribution from the common gate transistor is directly referred to the input terminal, which results in worsening the input referred current noise and makes it unsuitable for low noise TIA design.
- Also, to reduce thermal noise R_D needs to be increased which is limited by the lower voltage headroom available in newer technology and hence, high thermal noise is also present in the system.

- Input referred noise current expression becomes worse when all parasitic capacitances are taken into account at high frequencies.

High input referred noise current is the primary reason to look for other topologies. As a result, resistive feedback topology has been investigated to counter the drawbacks of the common gate topology.

2.3 Resistive Feedback



2.3.1a Motivation: Since, the common gate configuration limits maximizing R_D due to voltage headroom constraints, resulting in poor noise performance; feedback topology can be utilized to help in maximizing feedback resistance without having constraints for voltage headroom; as shown in figure (on the left).

2.3.1b Gain: The transimpedance gain of the system can be determined to be equal to:

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{i_{sig}}} \approx -\frac{\boldsymbol{A}}{\boldsymbol{(1+A)}} \frac{\boldsymbol{R_F}}{\boldsymbol{1+\left(\frac{R_F C_P}{A+1}\right)s}}$$

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{i_{sig}}} \approx -\boldsymbol{R_F}$$

- Thus, Trans impedance gain at low frequency is given by, $A_v \approx -R_F$. Clearly, increasing the value of R_F results in increasing the gain of the design. Since, R_F do not carry large current, it can be increased to increase the closed loop gain compromising on sensitivity (smaller loop gain); but helps in designing TIA with low input current noise due to the large resistor.

2.3.1c Bandwidth: Shunt-shunt feedback reduces the Input impedance, by the gain of the amplifier. If the amplifier contributes pole at very high frequencies, then the bandwidth of the system can be written as,

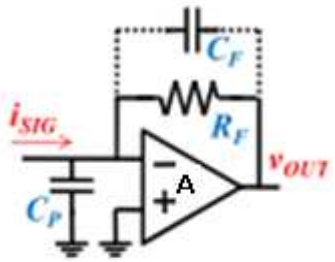
$$w_{3db} = \frac{A}{(R_F(C_P + C_F))}$$

Where, C_F is the feedback capacitance in parallel to R_F introduced, to obtain maximally flat response.

Note: However, if the TIA is being designed for MEMS resonators for GSM communication, then the required bandwidth will be 800MHz-1GHz. Since, the required bandwidth is pretty large, the poles due to opamp will become significant in determining the bandwidth of the TIA. Hence, the above mentioned simplifications may not be appropriate and requires in-depth analysis of the opamp, while taking into account the bandwidth of the opamp.

2.3.1d Bandwidth Analysis

Considering, BW as the bandwidth of the opamp and A_o as the gain of the opamp, the expression for the transimpedance of the system can be written as,



$$\frac{v_{out}(s)}{i_{SIG}(s)} = -\frac{R_F}{1 + \frac{s}{w_o Q} + \frac{s^2}{{w_o}^2}}$$

Where,

$$w_o Q = \frac{A_0 BW}{R_F(C_P + A_o C_F)BW + 1}$$

and,

$$w_o{}^2 = \frac{A_0 BW}{R_F(C_P + C_F)}$$

For the Maximally Flat Response: $w_{3db} = w_o$

Now, for system to have no ringing the relation for the w_o can be determined and bandwidth of the system can be approximated as,

$$w_{3db}{}' = \frac{\sqrt{2}A}{(R_F(C_P + C_F))}$$

Remark: The bandwidth is greater than that of the 1st order topology as analyzed in previous section, by about 41% because the pole introduced by the core amplifier creates an inductive behavior in the input impedance of TIA; partially cancelling the roll-off due to the input capacitance.

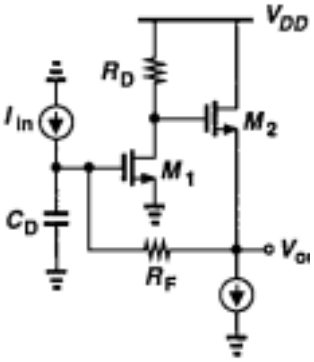
2.3.1e Noise Analysis: Considering the noise current contribution by the opamp and the resistor, the input referred noise current can be determined. Noise current of the opamp is neglected (very small) in comparison to other significant noise contributing sources. Input referred Noise current can be written as,

$$\overline{\imath_n{}^2} \approx \frac{4kT}{R_F} + (\frac{1}{R_F} + w^2(C_P + C_F)^2)\overline{v_{n_{opamp}}{}^2}$$

Clearly, value of R_F needs to be increased to minimize the noise contribution because of it. However, increasing R_F results in increasing the gain but narrowing down the bandwidth of the design. Also, voltage noise contribution from the opamp can be significantly large, resulting in exploring various topologies implementing shunt-shunt resistive feedback.

2.3.2 Topologies implementing Resistive Feedback

2.3.2a Resistive Feedback from Source Follower



Shunt-shunt resistive feedback from the source follower stage is being implemented in the design. The source follower isolates the R_D from the loading effect of both R_F & input capacitance of the subsequent stage. Value of R_F can be maximized to minimize noise and to increase gain as it does not limit headroom constraints.

Gain: The gain of the amplifier is given by,

$$A_v \approx -\frac{g_{m1}R_D}{(1 + g_{m1}R_D)}R_F \approx -R_F$$

Bandwidth: Since, input parasitic capacitance is very large (~1pF) the dominant pole is determined on the input side and hence, equivalent input resistance determines the bandwidth of the design. Now, the input resistance is given by,

$$R_{in} \approx \frac{R_F}{(1 + g_{m1}R_D)}$$

Hence, bandwidth is given by,

$$w_{3db} = \frac{(1 + g_{m1}R_D)}{C_P R_F}$$

Noise: To determine the input referred noise current, initially the output referred voltage noise is determined and then is being divided by the gain of the topology to fetch input noise current.
Now,

$$\overline{v_{n,out}{}^2} \approx 4kT\gamma g_{m1}R_D{}^2 + 4kTR_D + 4kT\frac{\gamma}{g_{m2}}$$

Hence, input referred voltage noise is given by,

$$\overline{v_{n,in}{}^2} \approx \frac{v_{n,out}{}^2}{(g_{m1}R_D)^2} \approx 4kT\frac{\gamma}{g_{m1}} + 4kT\frac{1}{g_{m1}{}^2R_D} + 4kT\frac{\gamma}{g_{m2}g_{m1}{}^2R_D{}^2}$$

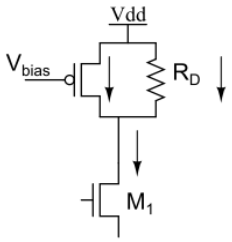
Now,

$$\overline{i_{n,in}{}^2} \approx \frac{4kT}{R_F} + \frac{\overline{v_{n,in}{}^2}}{R_F{}^2}$$

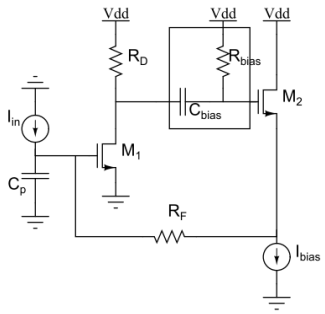
Hence, the input referred noise current is,

$$\overline{i_{n,in}{}^2} \approx \frac{4kT}{R_F} + \frac{4kT}{R_F{}^2}\left(\frac{\gamma}{g_{m1}} + \frac{1}{g_{m1}{}^2R_D} + \frac{\gamma}{g_{m2}g_{m1}{}^2R_D{}^2}\right)$$

Remark: It can be deducted from the noise expression, that for the given transimpedance gain only g_m and R_D can be maximized to minimize the noise. Various methods to achieve this can be:

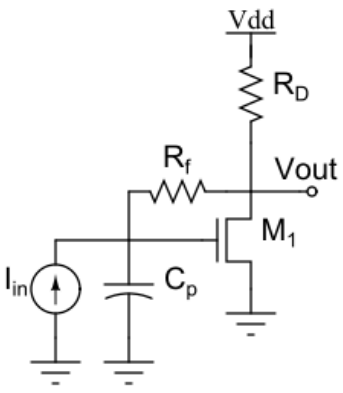


- Gain Boosting: Using pmos in parallel to R_D to maximize value of R_D and providing alternating path to the drain current. The new transistor may result in contributing it own high drain current noise nullifying the effect of increasing R_D to reduce its thermal noise. Hence, proper design consideration w.r.t noise analysis should be taken into account while designing.



- Capacitive Isolation: Capacitor can be introduced between the connecting path of M_1 and M_2. This helps in reducing the voltage headroom constraint on R_D and hence, value of R_D can be increased to reduce the thermal noise R_D. But, introducing capacitor results in lowering bandwidth and stability by introducing another dominant pole across R_D. Also, biasing circuit for M_2 may require resistors and hence, their thermal noise contribution adds to the noise of the system.

2.3.2b Resistive-shunt Feedback



As the technology scales, the voltage headroom becomes more and more limited resulting in smaller R_D and hence, higher noise current. Also, voltage headroom constraints limits the realization of source follower stage in the TIA design as described above. Hence, resistive shunt feedback topology is utilized which avoids source follower stage for the feedback.

Gain: The gain of the design is given by,

$$A_v \approx -\frac{(g_{m1}R_F - 1)}{(1 + g_{m1}R_D)}R_F \approx -R_F$$

Bandwidth: The input resistance is given by,

$$R_{in} \approx \frac{(R_F + R_D)}{(1 + g_{m1}R_D)}$$

And, hence bandwidth can be approximated as,

$$w_{3db} = \frac{(1 + g_{m1}R_D)}{C_P(R_F + R_D)}$$

Noise: The input referred noise current can be determined and the expression is given by,

$$i_{n,in}{}^2 = \frac{\overline{\iota_{n,M_1}{}^2} + \overline{\iota_{n,R_D}{}^2} + g_{m1}{}^2\overline{v_{n,R_F}{}^2}}{g_{m1}{}^2R_F{}^2}$$

Hence,

$$\overline{\iota_{n,in}{}^2} \approx (\frac{4kT\gamma}{g_{m1}R_F{}^2} + \frac{4kT}{g_{m1}{}^2R_F{}^2R_D} + \frac{4kT}{R_F})$$

Remark: The noise contribution do not have terms because of source follower as in previous case and hence, lower noise current and higher sensitivity.

Comparison with Resistive Feedback with Source Follower: *Resistive-shunt feedback* has the same transimpedance gain as *resistive feedback with source follower* but higher input resistance and hence, lowers bandwidth. Moreover, the input referred noise contribution is smaller in resistive-shunt feedback.

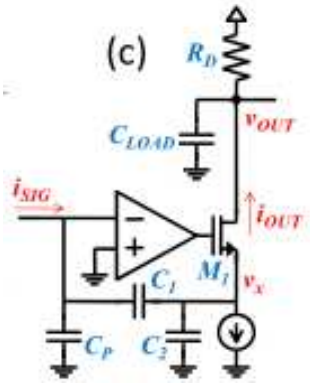
2.3.3 Why not use Switch Capacitors?

The substitution of the feedback resistor R_F with a switched-capacitor resistor cannot be used in context of high-sensitivity wide bandwidth applications. Since a clock frequency greater than the signal bandwidth is required to avoid aliasing effects, the charge injection during the switching becomes a critical parameter. For example, a clock frequency of 1GHz and a charge injection as low as 1fC give a spurious current of 1 uA!

3. Why to look for other topologies?

3.1 Motivation. In all the resistive feedback topologies as discussed above, design clearly tradeoffs among noise, gain and bandwidth. Large value of R_F is required for lowering noise and obtaining higher gain, which is being limited by on-chip maximum realizable resistance. Higher, value of R_F directly lowers down the bandwidth of the TIA. As a result, it becomes inevitable to introduce some degree of freedom in noise or bandwidth expressions by introducing other techniques such as capacitive feedback and integrator-differentiator approach as discussed below; which helps in complementing the gain of the TIA without involving large resistances. The idea is to achieve partial gain through noiseless capacitive gain.

3.1.1 Approach 1: Capacitive Feedback



Capacitive topology helps in generating the current within the design, enhancing the transimpedance gain of the TIA. In this topology the amplifier maintains a virtual ground at the input node and hence, i_{SIG} flows through C_1. Hence, C_1 senses the voltage across C_2 and returns a proportional current to the input. Hence, $v_x = -i_{SIG}/sC_1$. This voltage necessitates the current a current through C_2 ($=sv_xC_2$), which is supplied by source follower M_1. Consequently, the amplifier, M_1 with resistor R_D forms a TIA.

- If amplifier has a very high gain ($A_o >> 1$), then $I_{out}/I_{SIG} = (1+C_2/C_1)$. Circuit behaves as current amplifier and for resistance of R_D provides transimpedance gain of $(1+C_2/C_1)R_D$.
- The capacitive gain $(1+C_2/C_1)$ augments the gain of the resistor and allows for larger on-chip gain.
- Capacitive gain $(1+C_2/C_1)$ does not contribute noise. Further, noise current of R_D is divided by $(1+C_2/C_1)$.
- Gm enhancement due to feedback is present and hence pole on the source of M_1 is given by, $w_p \sim A_o g_m/2\pi C_2$. Hence, pole at source node is at high frequencies.
- The pole form $R_D C_{LOAD}$ appears outside the loop and do not determines the stability.

3.1.1a Gain: The gain of the topology is given by,

$$A_v \approx \left(1 + \frac{C_2}{C_1}\right) R_D$$

3.1.1b Bandwidth: since the required bandwidth is high, to compute the bandwidth of the system, poles due to opamp are taken into consideration, the analysis is as follows:

The transfer function for TIA gain can be computed as,

$$\frac{v_{out}(s)}{i_{SIG}(s)} = -\frac{R_D \frac{C_2}{C_1}\left(1 + \frac{s}{\frac{C_2}{C_1} A_0 BW}\right)}{1 + \frac{s}{w_o Q} + \frac{s^2}{{w_o}^2}}$$

Where,

$$w_o Q = \frac{C_1 A_0 BW g_m}{C_2(C_P + C_1)(BW + \frac{g_m}{C_2})}$$

And,

$${w_o}^2 = \frac{C_1 A_0 BW g_m}{C_2(C_P + C_1)}$$

To obtain a maximally flat response and ensure closed-loop stability, the equation can be simplified to obtain,

$$BW^2 \gg (\frac{g_m}{C_2})^2 \rightarrow \frac{g_m}{C_2} = \frac{(C_P + C_1)}{2C_1A_0}\, BW$$

$$w_{3db} = \frac{BW}{\sqrt{2}} = \frac{\sqrt{2}A_o g_m (C_1/C_2)}{(C_1 + C_P)}$$

3.1.1c Noise: The input referred noise current for the capacitive feedback topology is given by,

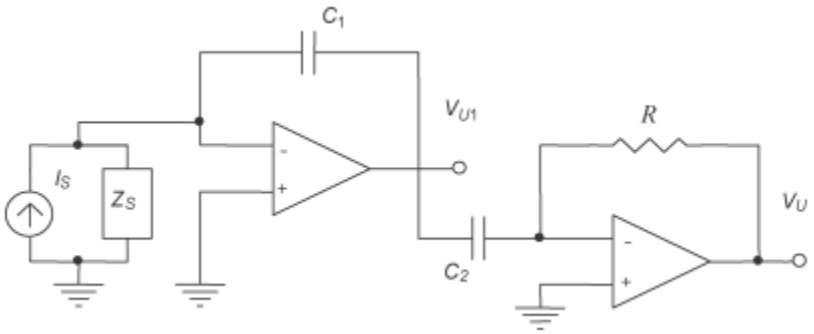
$$\overline{\iota_n{}^2} \approx \frac{4kT}{R_D(1+\frac{C_2}{C_1})^2} + (w^2(C_P + C_1)^2)\overline{v_{n_{opamp}}{}^2}$$

Note: Since, channel length modulation has been neglected in the analysis; there will be partial drain current noise contribution from the M_1 because of finite channel length modulation. Also, non-ideal biasing will result in noise (drain current noise because of biasing transistor).

Remark: The capacitive feedback TIA augments the gain of the resistor by the current gain ($1+C_2/C_1$) thereby allowing for larger on-chip gain. The noise from R_D is attenuated by ($1+C_2/C_1$) when referred to the input unlike resistive feedback where noise due to R_F is referred directly to the input.

3.2 Approach 2: Integrator – Differentiator Topology

3.2.1 Motivation: Since, the most important noise contribution in the bandwidth of the amplifier comes from the feedback resistor. The idea is to introduce completely reactive element for R_F i.e. introducing capacitor C_1, which doesn't contribute to the noise, resulting in gain of; A_{v1}=-1/ (j2πC_1). However, it is desirable to have a transimpedance gain that is independent of the frequency, which leads to the introduction of another stage with certain gain such that the overall transimpedance gain A_v is constant w.r.t frequency. Hence, the desired configuration has gain, A_{v2} = -j2πC_2A which leads to the design as shown in figure (on the left).



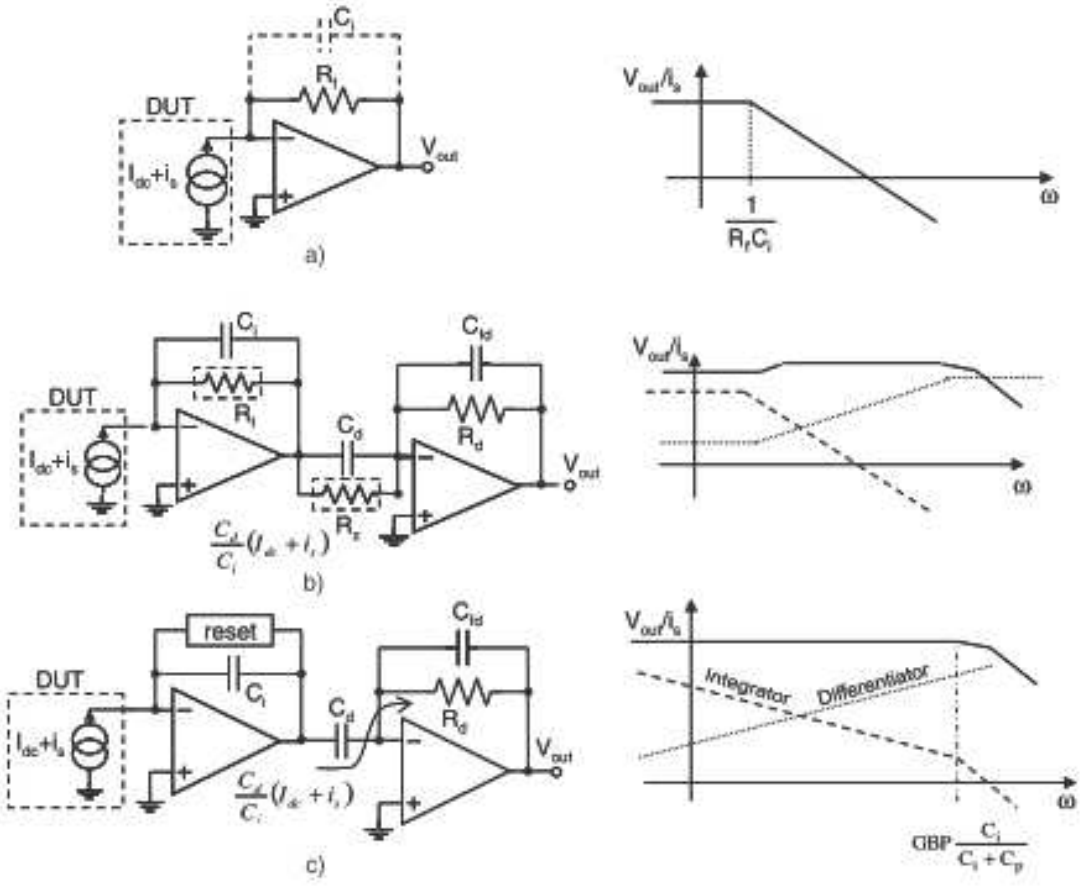
The overall gain of the system is given by,

$$A_v = -\frac{1}{j2\pi f C_1} * (-j2\pi f C_2 R) = \frac{C_2}{C_1} R$$

3.2.2 Comparison with Resistive Feedback Model

To compare the TIA gain of the topologies, the same value of low-frequency transimpedance gain is assumed, i.e.

$$A_v = -R_F = \frac{C_2}{C_1} R$$



The integrator-differentiator topology helps in improving the bandwidth of the system, as shown in figure (on the left). This shows that the topology helps in cancelling the pole-zero and increasing the bandwidth of the system.

The gain expression also shows that to obtain same transimpedance gain, the large ratio of C_2/C_1 can help in realizing large gain without using large value of resistor R; which is easy to be designed using on-chip resistance. This topology helps in increasing the transimpedance gain of the system by a factor of C_2/C_1 similar to the capacitive feedback topology discussed above. This topology also has the same benefits as capacitive feedback as it reduces the input

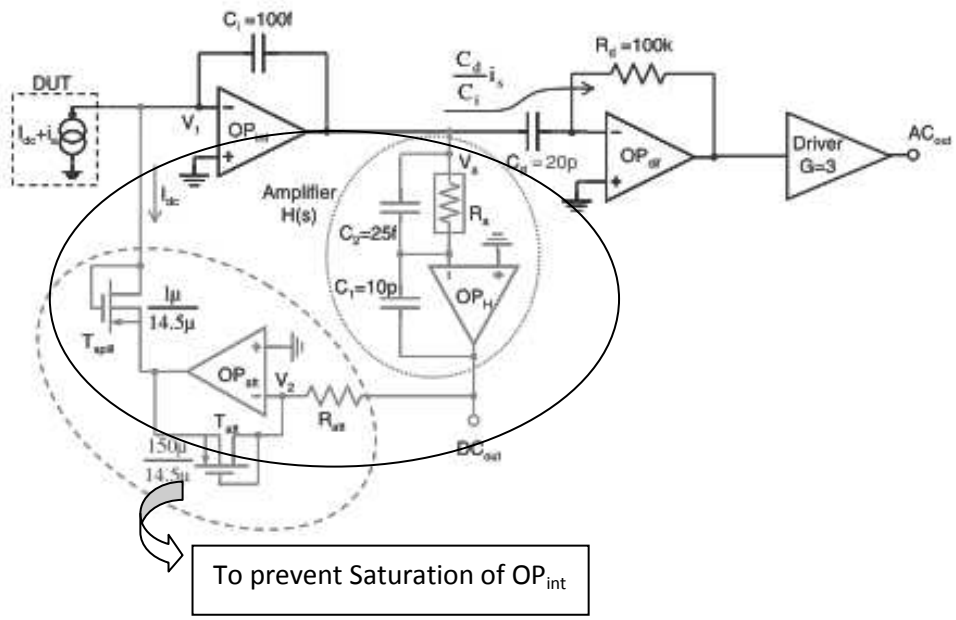
referred current noise because of thermal noise of R_D by the factor of (C_2/C_1).

Since, the design helps in achieving similar gain and lower noise with smaller resistance; it helps in increasing the bandwidth of the system. However, this may hold only when the poles introduced by the actual frequency response of the op-amps occur at frequencies higher than that corresponding to the pole introduced by the parasitic capacitance in parallel to R. Although this is often the case when dealing with transimpedance gain higher than 100 MΩ, detailed analysis of the frequency response of the system including the poles introduced by the opamp becomes essential.

3.2.3 Noise. As in the capacitive feedback topology, this topology helps in reducing the thermal noise contribution of the resistor R_D. However, one of the drawbacks of the design is that it introduces input referred noise contribution because of the voltage noise of another opamp added for integrator stage. This may results in reducing the noise performance of the design. Moreover, there is an increase of the contribution of the equivalent input noise source of the first stage at higher frequencies due to the presence of C_1.

This architecture offers the trade-off in term of minimum noise (besides the OpAmp noise, along the signal path only the resistor R_D affects the input noise but reduced by the amplifying factor of $(C_2/C_1)^2$), of accuracy of the current-to-voltage conversion factor (the gain being given by the ratio of two capacitances) and of large bandwidth practically approaching the gain bandwidth product (GBP) of the OpAmp.

3.2.4 Topology implementing Integrator-Differentiator



- Wide bandwidth and high sensitivity in current detection.

Bandwidth: Typically, the bandwidth of the circuit is given by;

$$w_{3dB} = A_0 BW.\frac{C_i}{(C_i + C_s)}$$

- To obtain high Bandwidth, C_i can be chosen of the order of C_s.

To increase Sensitivity: Reduce C_d. (Current in Differentiator = $\frac{C_d}{C_i} i_s$).

The issue with the topology is that the feedback capacitance of the integrator stage, C_i must be discharged to prevent its saturation due to the input leakage current. To prevent saturation, MOSFET switch is placed in parallel with the integrator capacitor C_i, which discharges it when the output voltage reaches a defined threshold. Similar design has been implemented [2] as shown on figure (on the left) for the continuous discharging of C_i to prevent saturation.

Noise: The input referred noise current can be determined for the system by including all relevant noise sources resulting in,

$$\overline{\iota_n{}^2} \approx \frac{4kT}{R_{att}M^2} + \overline{\iota_{Tspill}{}^2} + w^2(C_i + C_s)^2\overline{v_{n_{opint}}{}^2} + (\frac{C_i}{C_d})^2\frac{\overline{v_{n_{opdiff}}{}^2}}{R_D{}^2} + \frac{4kT}{R_D(C_d/C_i)^2}$$

Where, M is the ratio of the size of T_{att}/T_{spill} (~100); which results in very low noise contribution from R_{att}.

4. Comparison of Capacitive Feedback with Integrator-Differentiator Approach

For the equal transimpedance gain of both the topologies, the input referred noise contribution of capacitive feedback is lower as compared to integrator-differentiator.

Integrator-Differentiator:

$$\overline{\iota_n{}^2} \approx \frac{4kT}{R_{att}M^2} + \overline{\iota_{Tspill}{}^2} + w^2(C_i + C_s)^2\overline{v_{n_{opint}}{}^2} + (\frac{C_i}{C_d})^2\frac{\overline{v_{n_{opdiff}}{}^2}}{R_D{}^2} + \frac{4kT}{R_D(C_d/C_i)^2}$$

Capactive Feedback:

$$\overline{\iota_n{}^2} \approx +(w^2(C_P + C_1)^2)\overline{v_{n_{opamp}}{}^2} + \frac{4kT}{R_D(1+\frac{C_2}{C_1})^2}$$

Almost equal

In integrator-differentiator topology, the noise contribution from the voltage noise of 2nd opamp (differentiator) and also the noise due to RESET system increases the overall noise of the topology as compared to the capacitive feedback topology. Hence, may not be suitable for low noise applications. Also, the power consumption in integrator-differentiator is higher as compared to capacitive, because of more complex design and large overhead. The power results can be easily verified by comparing the results obtained from [1] & [2].

5. Biasing Issue

One of the major challenges in designing the capacitive feedback topology and the integrator-differentiator topology, is to bias the TIA. Only capacitive feedback and no DC path to the nodes can result in drifting of the node voltages which ceases the functionality of the TIA. Resistor cannot be introduced in parallel to the capacitor in both the topologies, as it will introduce its own thermal noise and requires large value of resistor to minimize it. In Capacitive feedback topology, differential TIA realization becomes necessary to provide DC path to the nodes as shown in [1] and helps in improving the performance of the TIA.

The other constraint in designing such low noise TIAs is to minimize the biasing noise of the amplifier. These topologies in practical systems at times are limited by the biasing noise and hence, biasing them becomes as important aspect of designing.

6. Summary

In depth study of various topologies for high gain, high bandwidth TIA design being implemented in various applications ranging from optical transceivers to nano-bio sensors has been done and various trade-offs while designing has been determined. Depending upon the constraints/specifications of the design particular topology can be considered.

It has been concluded that TIA implementation for the MEMS resonators in GSM communications can be done using capacitive feedback techniques in place of shunt-shunt resistive feedback to minimize input noise. Integrator-differentiator topology adds lot of overhead in comparison to the capacitive feedback technique. Resistive feedback and capacitive feedback are suitable options to be implemented. For very noise applications capacitive feedback provides better performance and high gain. However, while using capacitive feedback; noise due to biasing design should also be considered. The results obtained for the gain, bandwidth and noise for various topologies has been listed down in the

section and it can be seen that the shunt-shunt resistive feedback and capacitive feedback topologies have very competitive figures and careful study is required for particular application and specifications.

7. Detailed Analysis

7.1 Noise Analysis

Design	Input Referred Current Noise, $\overline{\imath_n^2}$
Integrator-Differentiator	$\overline{\imath_n^2} \approx \frac{4kT}{R_{att}M^2} + \overline{\imath_{Tspill}^2} + w^2(C_i + C_s)^2\overline{v_{n_{opint}}^2} + (\frac{C_i}{C_d})^2\frac{\overline{v_{n_{opdiff}}^2}}{R_D^2} + \frac{4kT}{R_D(C_d/C_i)^2}$
Capacitive Feedback	$\overline{\imath_n^2} \approx \frac{4kT}{R_D(1+\frac{C_2}{C_1})^2} + (w^2(C_P + C_1)^2)\overline{v_{n_{opamp}}^2}$
Resistive Feedback-opamp	$\overline{\imath_n^2} \approx \frac{4kT}{R_F} + (\frac{1}{R_F} + w^2(C_P + C_F)^2)\overline{v_{n_{opamp}}^2}$
Resistive Feedback with Source Follower	$\overline{\imath_{n,in}^2} \approx \frac{4kT}{R_F} + \frac{4kT}{R_F^2}(\frac{\gamma}{g_{m1}} + \frac{1}{g_{m1}^2R_D} + \frac{\gamma}{g_{m2}g_{m1}^2R_D^2})$
Resistive Shunt Feedback	$\overline{\imath_{n,in}^2} \approx (\frac{4kT\gamma}{g_{m1}R_F^2} + \frac{4kT}{g_{m1}^2R_F^2R_D} + \frac{4kT}{R_F})$
Cascode Topology	$\overline{\imath_n^2} \approx \frac{4kT}{R_B} + \frac{4kT}{R_D} + 4kT\frac{2}{3}g_{m3} + 4kT\frac{2}{3}g_{m4} + 4kT\frac{2}{3}g_{m5} + \frac{8kT}{3g_{m3}(z_{in}^2)}$
Common Gate	$\overline{\imath_n^2} \approx \frac{4kT}{R_D} + 4kT\gamma g_{m2}$

7.2 Gain Analysis

Design	Transimpedance Gain, Av
Integrator-Differentiator	$A_v \approx -\frac{C_d}{C_i}R_D$
Capacitive Feedback	$A_v \approx -\left(1+\frac{C_2}{C_1}\right)R_D$
Resistive Feedback-opamp	$\frac{v_{out}}{i_{sig}} \approx -\frac{A}{(1+A)}\frac{R_F}{1+\left(\frac{R_FC_P}{A+1}\right)s} \approx -R_F$
Resistive Feedback with Source Follower	$A_v \approx -\frac{g_{m1}R_D}{(1+g_{m1}R_D)}R_F \approx -R_F$
Resistive Shunt Feedback	$A_v \approx -\frac{(g_{m1}R_F-1)}{(1+g_{m1}R_D)}R_F \approx -R_F$
Cascode Topology	$A_v \approx -R_D$
Common Gate	$A_v \approx -R_D$

7.3 Bandwidth Analysis

Design	**Transimpedance Gain, Av**
Integrator-Differentiator	$w_{3db} \approx \frac{A_o BW C_i}{(C_i + C_p)}$
Capacitive Feedback	$w_{3db} \approx \sqrt{2}\frac{A_o g_m}{(C_i + C_p)}\left(\frac{C_1}{C_2}\right)$
Resistive Feedback-opamp	$w_{3db}{}' = \frac{\sqrt{2}A}{(R_F(C_P + C_F))}$
Resistive Feedback with Source Follower	$w_{3db} = \frac{(1 + g_{m1}R_D)}{C_P R_F}$
Resistive Shunt Feedback	$w_{3db} = \frac{(1 + g_{m1}R_D)}{C_P(R_F + R_D)}$
Cascode Topology	$w_{3db} = \frac{1}{2\pi g_{m1} g_{m4} R_B}$
Common Gate	$w_{3db} = \frac{1}{g_m C_p}$

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9. Literature Survey

Reference #	Technology	Gain	Bandwidth	Noise	Power	TIA Design
1.	0.18um	56Mohm = ~155dB	1.8 MHz	65fA/$\sqrt{Hz}$ - Input Referred	436 uW	Capacitive Feedback
2.	0.35um - 3.3V	25 Mohm = ~148dB	~1.5 MHz	4-5fA/$\sqrt{Hz}$ - Input Referred	21 mW	Integrator - Differentiator
3-F.Ayazi, Georgia	0.18um - 1.5V	64dB-76dB	1.7GHz-2.1GHz	~7pA/$\sqrt{Hz}$ - Input Referred	4.8mA*1.5V =7.2mW	Current Pre-Amplifier
4-Razavi	0.6um-3V	8.7kohm= 78.8dB	550Mhz	4.5pA/$\sqrt{Hz}$ - Input	30mW	Capacitive Feedback
5-Wang	0.18um	82dB	2.4GHz	36pA/$\sqrt{Hz}$	19.5mW	Wide Swing Cascode Topology
6-Sundaresan	0.18um				2.6mW	Folded Cascode OTA with Resistive(active) feedback followed by CS stage
7-Sundaresan	0.5um		Gain*BW= 175 MHz		1.8mW	Folded Cascode OTA with Resistive(active) feedback
8-A. Kopa	0.18um	64dB	2 GHz	4.2 pA/$\sqrt{Hz}$	10.7mW	Common Source Feedback
9-Wei chen	0.18um	87dB	7.6GHz		210 mW	Gm enhancement, Resistive feedback TIA
10-C. Nguyen	0.35um-1.65V	8kohm-78dB	200MHz		350uW	Differential CMOS amp