Spring – 2009-10

EE314 – Midterm Design Project

High Frequency Transceiver LNA-Mixer Design

Submitted by

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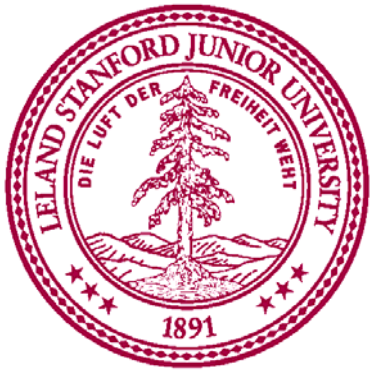
On

May 28th, 2010



1. SPECIFICATIONS TABLE

Specifications	**Design Objective**	**Design Results**
Frequency of Operation	Central Frequency: 2.45 GHz Frequency Range: 2.25GHz – 2.65GHz	Central Frequency: 2.5 GHz Frequency Range: 2.25GHz – 2.65GHz
Power Gain	>30db (over entire band)	>30db over given Frequency band, Peak Gain: 32.9dB
Spot Noise Figure	<2.5dB	~0.4dB
Power Consumed	Minimize	26mW
IIP3	>1dbm	-28dbm
Total Capacitors used	<300pF	MOSCAP #2 - 200u*200u (PMOS): 400pF each #2 - 250u*250u (PMOS): 416pF each Total # of MOSCAPS = 4 MIMCAPS None
Total Resistances used	<300K	84.14K
Total Inductors used	--------	Spiral Inductor (4+4) +(8+8) = 24nH Bondwire (0.6+0.6) + (3.9+3.9) = 9nH

2. **SCHEMATIC**

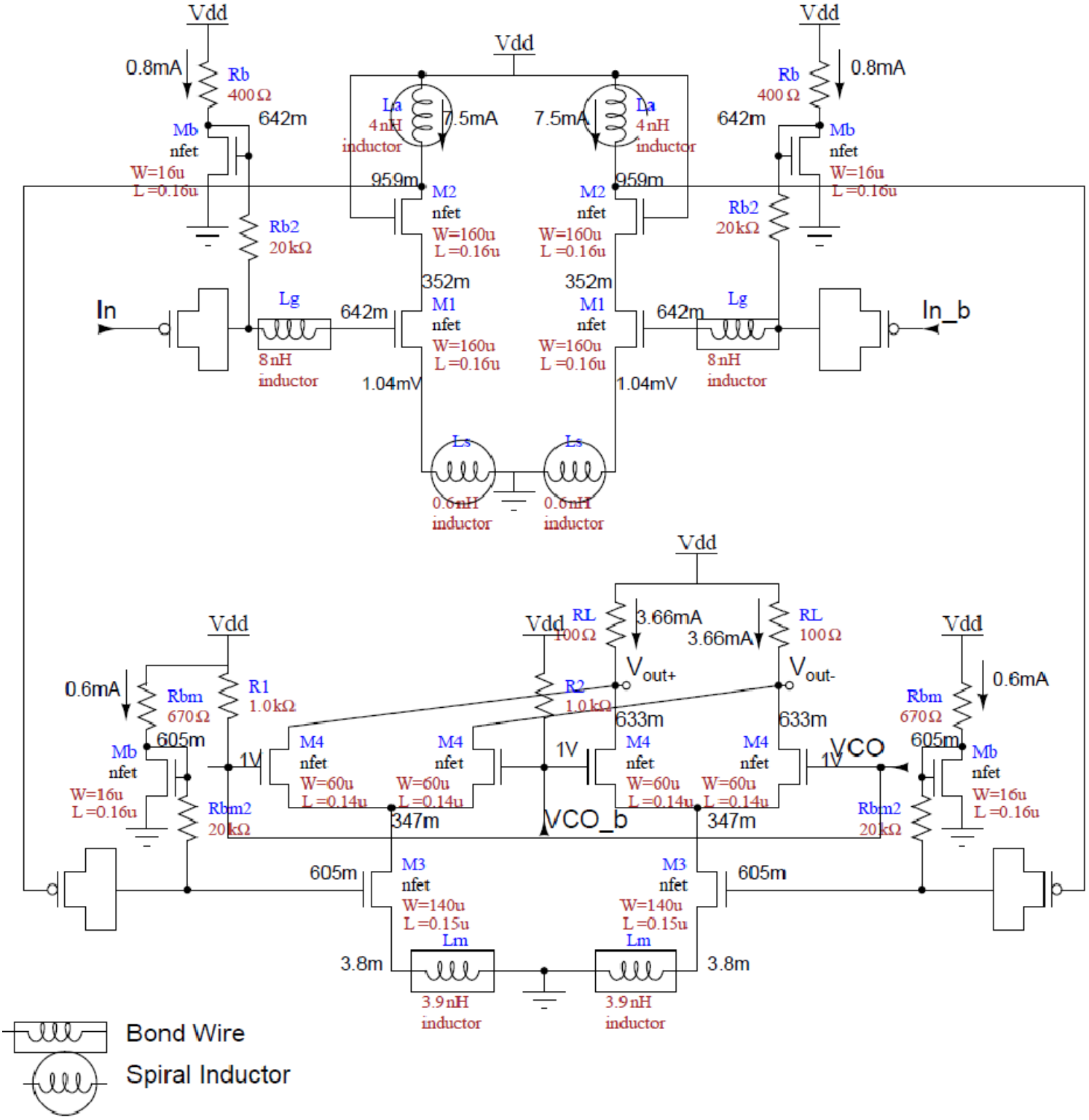


***Fig*1.** Complete Schematic Design of LNA – Mixer

3. NETLIST

```
subckt frontend_ee314 In In_b Out Out_b VCO VCO_b vdd gndall inh_bulk_n
   I67 (net141 transistor_in) ind_bondwire _par0=1 length_in_mm=5
   I66 (net73 net109) ind_bondwire _par0=1 length_in_mm=5
   I56 (net75 gndall) ind_bondwire _par0=2 length_in_mm=4.75
   I57 (net107 gndall) ind_bondwire _par0=2 length_in_mm=4.75
   M78 (gndall net80 net80 inh_bulk_n) cmosn_ee314 w=16u l=160n
   M77 (gndall net83 net83 inh_bulk_n) cmosn_ee314 w=16u l=160n
   M76 (gndall net86 net86 inh_bulk_n) cmosn_ee314 w=16u l=160n
   M75 (net104 VCO Out_b inh_bulk_n) cmosn_ee314 w=60u l=140n
   M74 (net93 vdd cascode_in inh_bulk_n) cmosn_ee314 w=160u l=160n
   M73 (cascode_in transistor_in net95 inh_bulk_n) cmosn_ee314 w=160u \
      l=160n
   M72 (net75 RF_b net116 inh_bulk_n) cmosn_ee314 w=140u l=150n
   M71 (net116 VCO_b Out_b inh_bulk_n) cmosn_ee314 w=60u l=140n
   M69 (Out VCO_b net104 inh_bulk_n) cmosn_ee314 w=60u l=140n
   M70 (net104 RF net107 inh_bulk_n) cmosn_ee314 w=140u l=150n
   M68 (net111 net109 net110 inh_bulk_n) cmosn_ee314 w=160u l=160n
   M66 (net152 vdd net111 inh_bulk_n) cmosn_ee314 w=160u l=160n
   M67 (Out VCO net116 inh_bulk_n) cmosn_ee314 w=60u l=140n
   M65 (gndall net137 net137 inh_bulk_n) cmosn_ee314 w=16u l=160n
   R72 (RF_b net80) resistor r=20K
   R71 (net80 vdd) resistor r=670
   R70 (net141 net83) resistor r=20K
   R69 (net83 vdd) resistor r=400.0
   R68 (RF net86) resistor r=20K
   R67 (net86 vdd) resistor r=670
   R66 (vdd VCO_b) resistor r=1K
   R65 (vdd VCO) resistor r=1K
   R64 (net73 net137) resistor r=20K
   R63 (net137 vdd) resistor r=400.0
   I65 (net141 net141 In net141) pmos4_ee314 Width=200u Length=200u
   I64 (RF RF net93 RF) pmos4_ee314 Width=250u Length=250u
   I63 (RF_b RF_b net152 RF_b) pmos4_ee314 Width=250u Length=250u
   I62 (net73 net73 In_b net73) pmos4_ee314 Width=200u Length=200u
   I61 (net95 gndall) ind_spiral_ee314 _par0=1 w=30u _par1=70u _par2=4u
   I60 (vdd net93) ind_spiral_ee314 _par0=1.8 w=26u _par1=550u _par2=2u
   I59 (net110 gndall) ind_spiral_ee314 _par0=1 w=30u _par1=70u _par2=4u
   I58 (vdd net152) ind_spiral_ee314 _par0=1.8 w=26u _par1=550u _par2=2u
ends frontend_ee314
```

4. DETAILED ANALYSIS

4.1 Introduction

The project dealt with designing the analog front end (LNA & Mixer) for a wireless receiver. The designing of the system involved tradeoff between noise figure, gain, linearity and power consumption. The goal while designing LNA is to achieve good input power matching and simultaneously minimum noise figure. While, the mixer is designed to obtain good linearity with suitable gain; without compromising on noise figure.

Since, the given specifications require large power gain and low noise figure; after investigating various topologies, we decided to use inductively degenerated cascoded design for the LNA and inductively degenerated double balanced active configuration for the mixer.

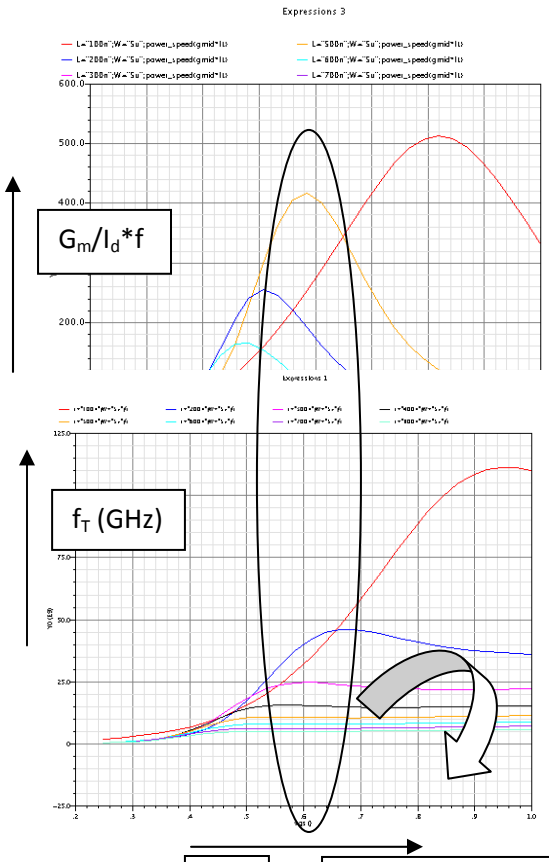
4.2 LNA Design

We followed the power constrained design approach for minimizing noise figure and achieving input matching simultaneously while designing LNA along with cascoded topology to minimize input-ouput interaction.

- For minimum noise figure, Q ~ 4.5- 6.5. This gives the approximate estimate of required Cgs as,

$$Cgs = \frac{1}{(2 * wo * Rs * Q)}$$

  Here, Rs= 100 Ohms, w_o= 2.45GHz. This results Cgs ~ 90fF.
- This value of Cgs can be used to estimate the optimum width for LNA input transistor as:



$$W_{opt} = \frac{1}{3*Wo*L*Cox*Rs}$$

Now, to determine the value of L (length of transistor) we characterized the transistors and generated gm/Id *ft vs. Vov curves for various values of L as shown in figure (on the left).

To get suitable Vov (considering the cascade topology) and high ft, we decided to operate at ~ 340mV.
Next, Cox was found using:

$$Cox = \frac{eox}{tox}$$

Where tox = 2.8nm as, 3.16* 1e-3 F/um^2.
Thus, putting in these values we get **Wopt = 169u**.

We decided to operate at **W=160u**.

Input Matching

- Ls is determined using the **net input impedance** looking into the transistor (neglecting effect of Cgd):

$$Input\ Impedance\ at\ LNA \approx \frac{1}{s(Cgs)} + s(Ls + Lg) + w_t * L_s$$

This clearly indicates that for power matching we need to equate the real part of the above equation to input resistance Rs =100Ω. This gives us value of Ls = 0.3nH. We verified the calculation by simulating our design.

Observation: However, when we simulated this value, we found discrepancies with this formula as the real impedance was ~ 50Ω inplace of 100Ω. This discrepancy was because of Cgd due to miller effect and hence, the required inductance of the design was increased to ~ 0.6nH. The new results were verified by obtaining input impedance curves of design (See page 16).

Realizing Ls: Since, we are using high f_T for designing, we determined that required inductance is very small for input power matching ~ (less than 1 nH); we quickly realized that spiral inductors can only be utilized with maximum Q_{ind} possible (to minimize inductor resistance that directly gets referred to the input with (1+β) factor and hence, also results in input impedance phase change and high noise figure). Thus, in order to determine the optimum values of n,w,Dout, s required for the spiral inductor we used MATLAB script (Appendix2:pp12) using following formulas:

$$Din = Dout - 2 * n * w - 2(n-1) * s$$

$$\rho = \frac{Dout - din}{Dout + Din}$$

$$Rs = l/(w * \sigma * \delta * (1 - e^{\frac{-t}{\delta}})$$

$$Cp = n * w^2 * \frac{eox}{tox}$$

$$\frac{Cox}{2} = l * \frac{eox}{2} * [\frac{w}{tox} + 0.77 + 1.07 * [(\frac{w}{tox})^{0.25} + (\frac{t}{tox})^{0.5}]$$

The final values for the 4 parameters used were: n= 1, Dout= 70u, s=4u, w= 30u.
NOTE: Calculations has been shown on page 9 in next section.

Cascode Transistor Sizing

This was decided by keeping the noise and gain tradeoff in mind as described in the text book. Keeping higher width would give us more noise while lesser width would give us worse input matching but helps in smaller input-output interaction with smaller Cgd contribution. Hence, we decided to keep the size of cascode transistor same as that of input transistor of LNA.

- **Output LNA Inductor Design**

The inductor La was really tricky to design. This is because it sees parasitic caps as Cgd of cascode transistor and Cgs of capacitor from the mixer input transistor. However, using a spiral over here would bring some more parasitic caps into picture as well. Also, the inductively degenerated mixer would introduce its own inductance looking into the gate of the mixer, further complicating this analysis. Hence, to include such parasitic effects we estimated the total capacitive load on output including mixer by estimating the widths of the mixer (As described in next section). The effective load was computed and for efficient power matching the optimum load inductance was determined. Hence we decided to assume the caps looking into La as ~ 350fF. This gave us the value of La for resonance at 2.45GHz as ~ 4.5nH. Another important consideration here is deciding the resistor for this inductor. As this is the gain resistor, we need to have a low Q inductor here. Hence using a spiral inductor here makes sense in order to get high gain. This time we tweaked the earlier MATLAB script to give high Rs and found the 4 parameters.

Remark: We used La final value as 4nH in our schematic after adjusting for power matching. The 4 parameters used were n= 1.8, Dout = 550u, s = 2u, w= 26u.
NOTE: Calculations has been shown on page 9 in next section.

- **Gate Inductor**
  This value is given simply by the resonance condition at w_o= 2.45GHz. The Cgs and the Cgd (miller attenuated) of the RF input transistor. Thus,

$$L_g = \frac{1}{w_o^2 * C_{tot}}$$

Which gives Lg= 8.44nH for Ctot ~ 500fF. We have taken the margin here for additional capacitors coming into picture from the spiral inductor in the source. Since a spiral inductor at this critical node would bring a number of parasitic caps making matching at 2.45GHz difficult to achieve, we used a bondwire of length 5mm and n=1 wire. These values were found from the calculations:

$$Inductance_{Bondwire} = \frac{length + 3}{n}$$

$$Resistance_{Bondwire} = \frac{0.31 * l + 0.6\sqrt{n}}{n}$$

Thus resistance at the gate due to the bondwire was 2.15 Ohms.

Remark: We used Lg ~ 8nH in our final design.
NOTE: Calculations has been shown on page 9 in next section.

4.3 MIXER DESIGN

To decide between the two mixer topologies i.e. active and passive, we considered the gain requirements of the system. We require a gain of 30db from the overall system. 30dB (= 1000 times) translates to a voltage gain 31.622 times. Gain of the LNA:

$$Gain_{LNA} = Q * g_m * R_{out}$$

$$Q = \frac{1}{2 * R_s} * \frac{w_t}{w_o}$$

$$Gain_{Mixer} = 2 * \pi * G_m * R_L$$

Since, the gain requirements were high and ballpark value of LNA gain being estimated was below the desired specifications, it became inevitable to achieve gain from mixer stage. This ruled out using a passive mixer completely. This gain analysis also helped us to find the approx. values of Gm as ~ 30e-3Ω^{-1}.

4.3.1 DESIGNING THE DOUBLE BALANACED

- **RF Transistors**: The RF differential pair is basically an LNA stage, and the transistors and associated passives can be optimized using the LNA design techniques i.e. inductive degeneration and input power matching. Another very important point here is that these transistors determine the linearity spec of the design to a large extent.

- **<u>Improving Linearity</u>**: Linearity of the mixer has been improved by increasing the inductor degeneration and to produce more linear transconductance. Also, the operating range of the mixer has been determined for the given specifications using the transient analysis. It has been observed that the variation in the input signal for RF ports is ~100mV peak-to-peak (for the given input voltage conditions). This requires constant gm for the given input range of small signal on the RF port for high linearity of the mixer.

  As shown in figure below, transconductance curve for the Rf transistor has been obtained at various operating voltages and various inductive degeneration. 1st order $(\frac{\partial Gm}{\partial Vgs})$ & 2nd order$(\frac{\partial^2 Gm}{\partial^2 Vgs})$ derivative of gm are also plotted (see graph below) to inspect (i)the nature of slope of gm, which should be zero in operating region and (ii) 3rd order non-linear term (to evaluate non-linearity). The width of the transistor has been obtained by evaluating suitable gain requirement and minimizing noise figure as done in case of LNA. As a result, length, L = 4nH and width, W = 140u has been used.

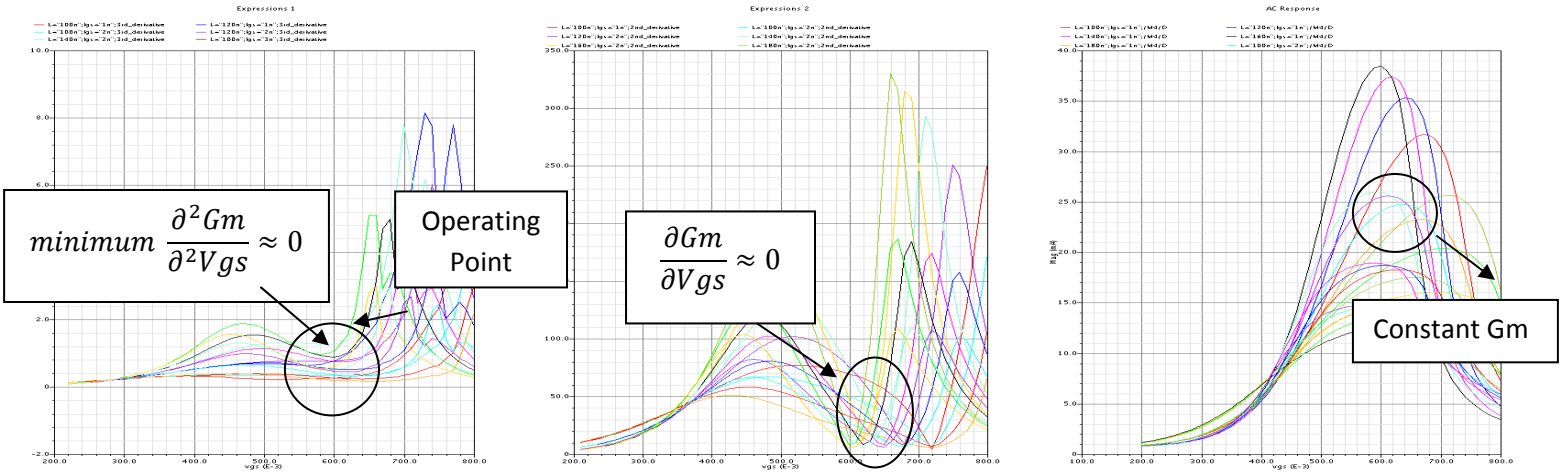


Fig. i) Second order derivative ii) First order derivative iii) Gm

REMARK: Inductance of 5nH was initially used in the design, but due to loading of stages, improper matching between LNA and mixer and intrinsic resistance of bond wire, to obtain required gain, inductance was reduced to ~4nH in the design. We chose Vgs = 0.6V with L = 4nH and gm= 25e-3.
Bondwire inductors were used for this with n=2 and length = 4.75mm.
<u>NOTE</u>: Calculations has been shown on page 9 in next section.

- **LO transistors:** These are sized so that they operate close to their peak f_T without contributing large drive capacitance (large width) at the bias current that is optimal for the differential pair transistors which is typically ~4-5 times smaller than RF transistor. We chose W= 60um for these in our final schematic. The length was chosen as 140n. It has also been ensured while deciding the width of LO transistor that not very high overdrive voltage is maintained so that the source node do not drop sufficient enough to drive RF transistor into linear region.

- **Biasing of the LO transistors:** While deciding the biasing of the RF transistor and width of the LO transistors, it is necessary to ensure that all the transistors operate in saturation region while the signal changes on RF port. As a result, the gate voltage on LO port, $Vg_{LO} > Vd_{RF} + Vt > Vg_{RF} + Vov_{LO}$. To maintain the required condition and to operate RF port at suitable bias so as to maximise transconductance and minimize non-linearity, LO node has been attached to 1V supply.

4.4 Observations and Conclusions

1. We tested the **individual LNA and mixer** units in order to get an idea of how is the power matching between the two stages. The gain and linearity curves for the same have been attached on pages 15-16. The IIP3 of the mixer alone was +4dBm and voltage gain of the LNA alone was 70.

2. **System Analysis:** The LNA interface with the Mixer was analyzed and it the final result shows that we have decent power matching with La design have Q_{La}~15. This results in R_p~1kΩ. On the mixer input the net impedance through simulation shoes ~ 620Ω. This reduces the gain of the LNA by ~1/2.

2. **L-Matching**: We tried to improve power matching between the stages using L match. Unfortunately, L-matching did not help much because of extra parasitic being introduced by it and changing the central frequency of the design and less degree of freedom. (Schematic attached below on pp. 20)

3. **Linearity Improvement:** We tried to use the "weak feed forward" method as described in lecture as we could afford to have slightly more noise and power dissipated. We chose N=1.1 and M= N^3= 1.33. However, we did not observe any improvement in linearity after using it possibly because the non-linearity introduced was much as compared to the mixer and hence, did not help in improving the linearity of the mixer. (Schematic attached below on pp.19).

4. **Other Designs**: While individually designing the two units, we came up with several designs which always seemed to tradeoff gain with linearity. Increasing the inductor L in the source of the mixer RF input transistor gave good linearity however reduced gain. An IIP3 curve from the design giving us highest linearity of -13dBm has been attached on page 21. Similarly a power gain curve from the design giving us gain of 36dB has been shown on page 21.

5. **Best Overall Design achieved**: We were able to come up with a design achieving >32 db gain over the given band while IIP3 of -15dBm. However, we were using bondwires of length > 5 mm for this purpose which violated the limitations specified.

4.5 Calculation Results

Parameters	Lg = 8nH	Ls = 0.6 nH	La = 4nH (Rf top)	Lm = 3.9nH (Mixer source)
Type	Bondwire	Spiral	Spiral	Bond Wire
Dout	----	70u	550u	----
n	----	1	1.8	----
S	----	4u	2u	----
W	----	30u	26u	----
Length (Bondwire)	5mm	----	----	4.75mm
N (Bondwire)	1	----	----	2
Din	----	0.1u	453u	----
ϱ	----	0.75	0.09	----
Cox	----	57.4fF	1300 fF	----
Rs	1.37Ω	0.1389 Ω	4.088Ω	1.34Ω

5. SIMULATION RESULTS

A) Summary of main results achieved from final design

1) Power Gain VS frequency

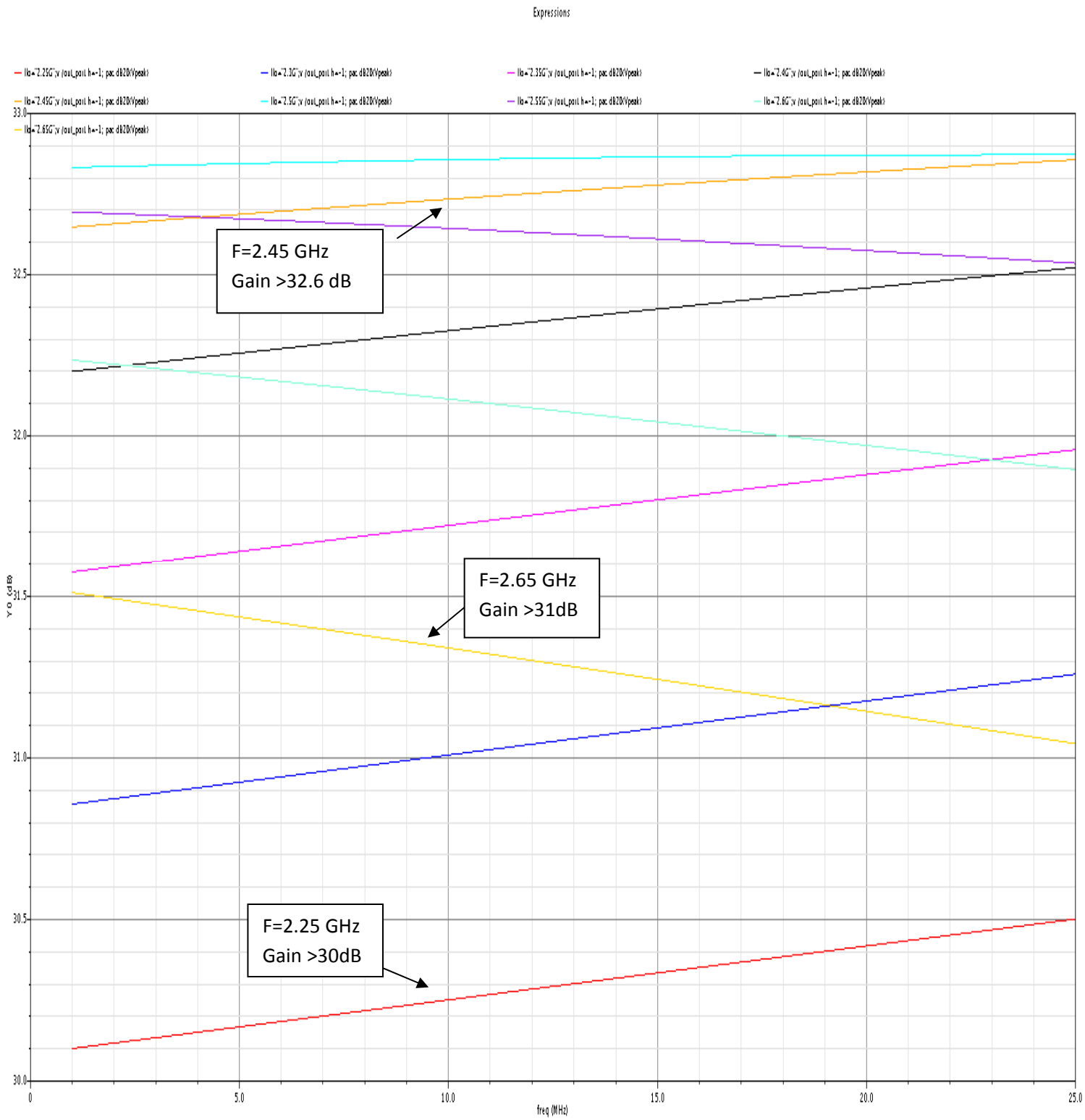


Fig. Power Gain vs. IF Frequency (MHz)

2) Noise Figure

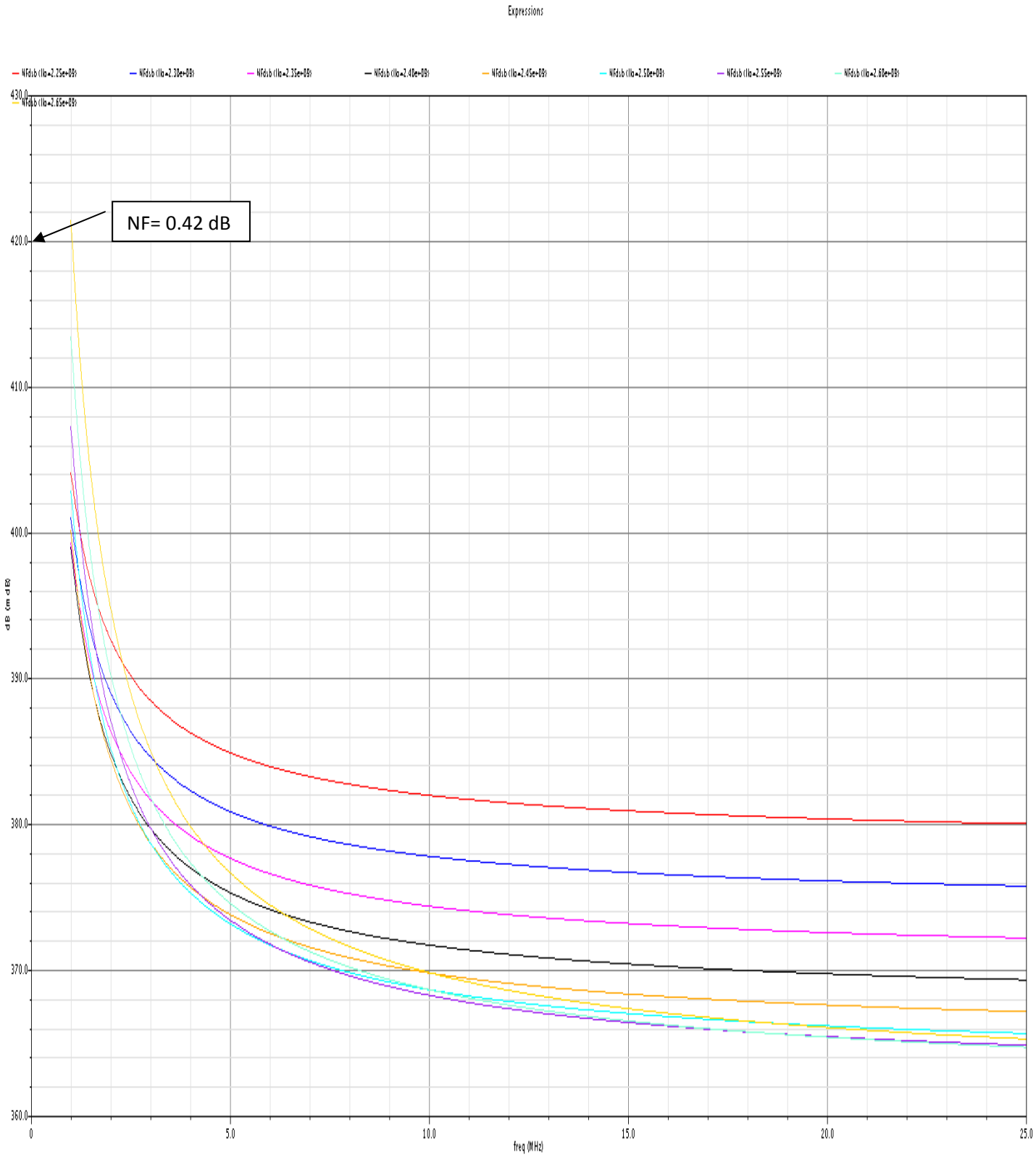


Fig. Noise Figure vs. IF Frequency (MHz)

3) **Power Dissipated**

(Shown in milliwatts on the y axis vs. frequency in GHz on the x axis)

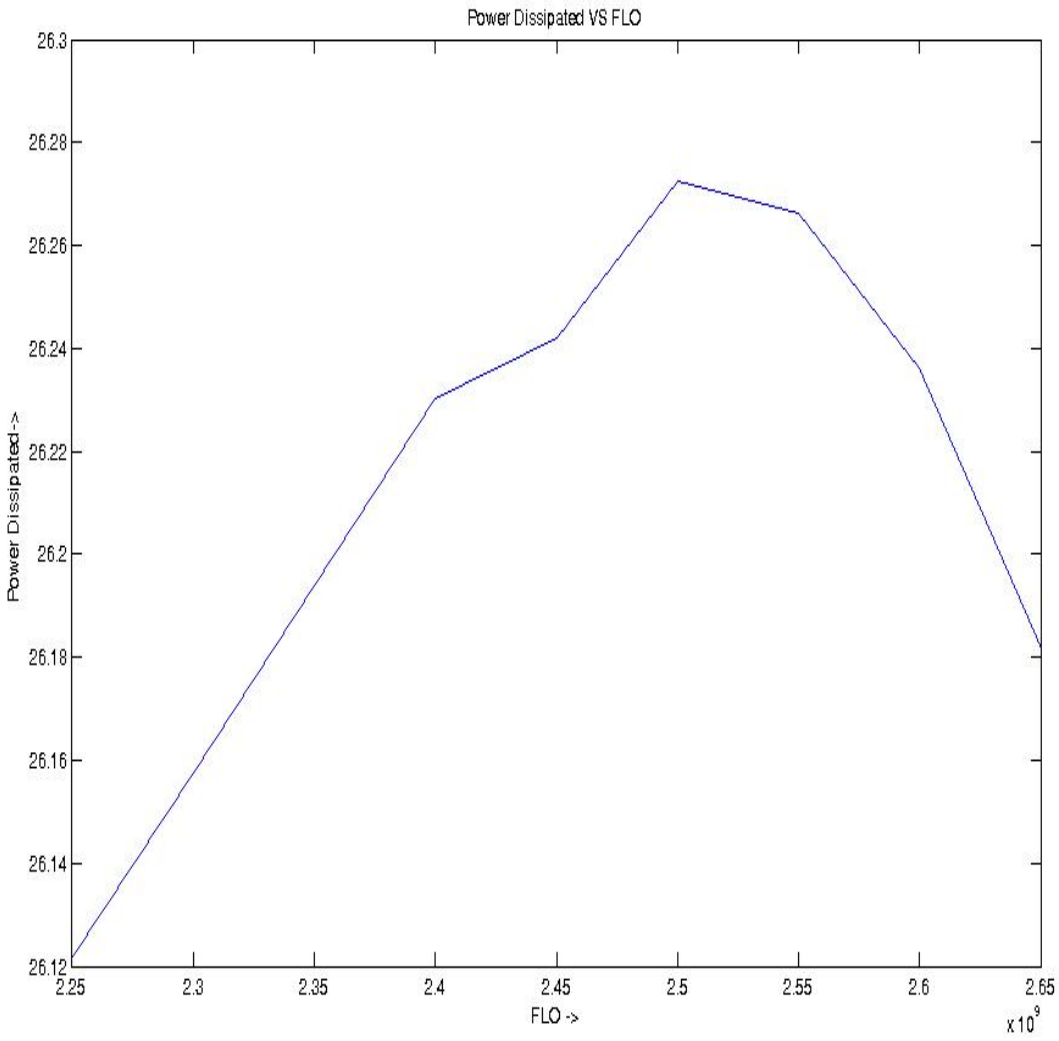


Fig. Power Dissipated (mW) vs. Frequency (GHz)

4) **3rd Order Input Intercept Point (IIP3) Curve**

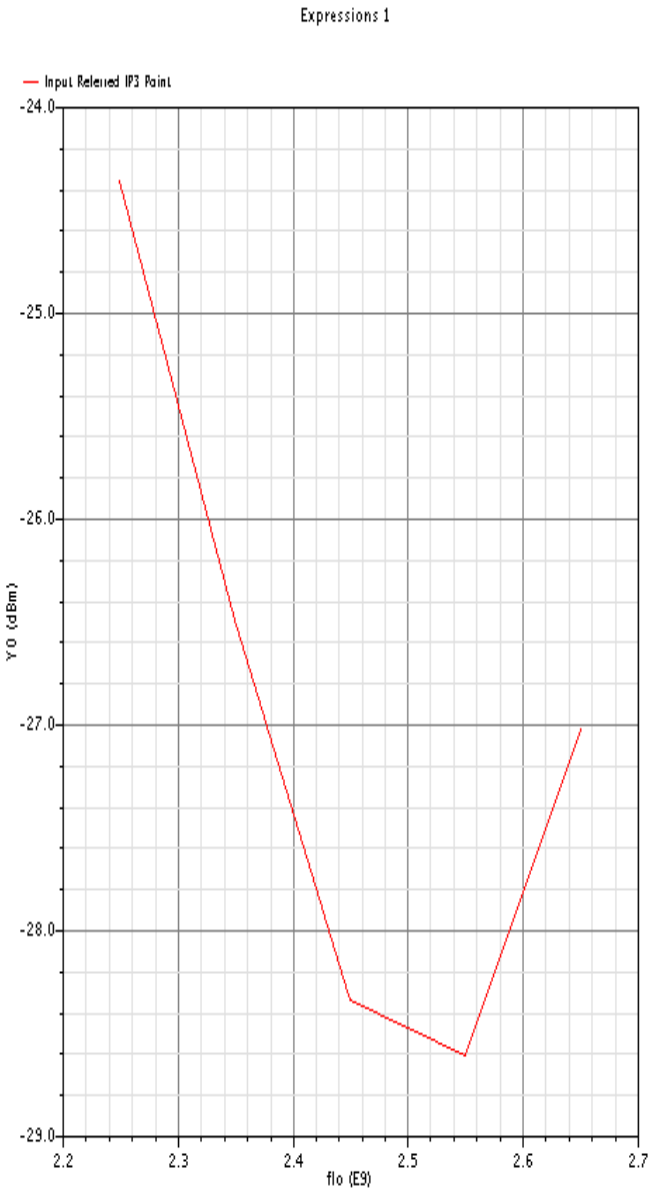


Fig. IIP3 (dBm) vs. Frequency (GHz)

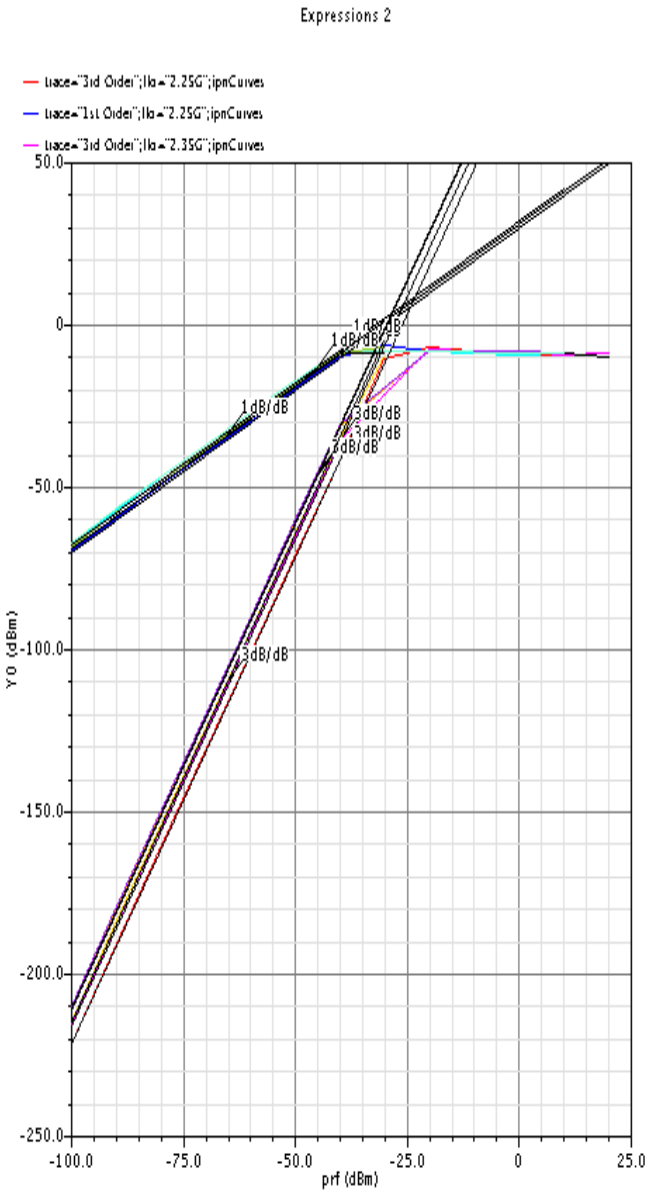


Fig. Power pf 3rd and 1st Harmonics as a function of input power for varying FLO

5) 1st and 3rd harmonic powers as a function of input power for FLO = 2.45G

IIP3 at 2.45GHz = -28.35dBm

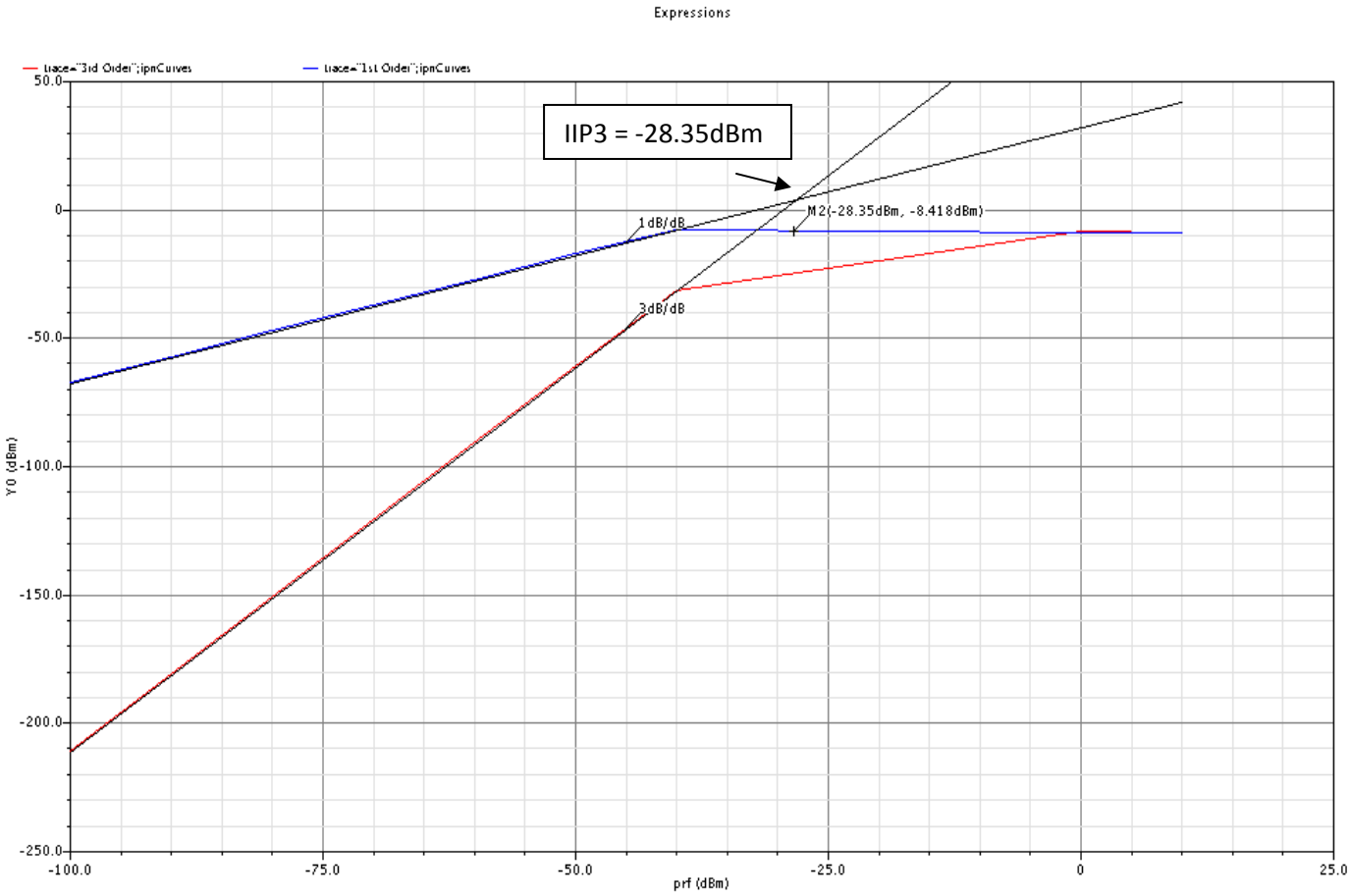


Fig. 1st and 3rd harmonic powers as a function of input power for FLO = 2.45G

B) Other important results

1. Gain of individual stages: (refer page 9)

i) Mixer

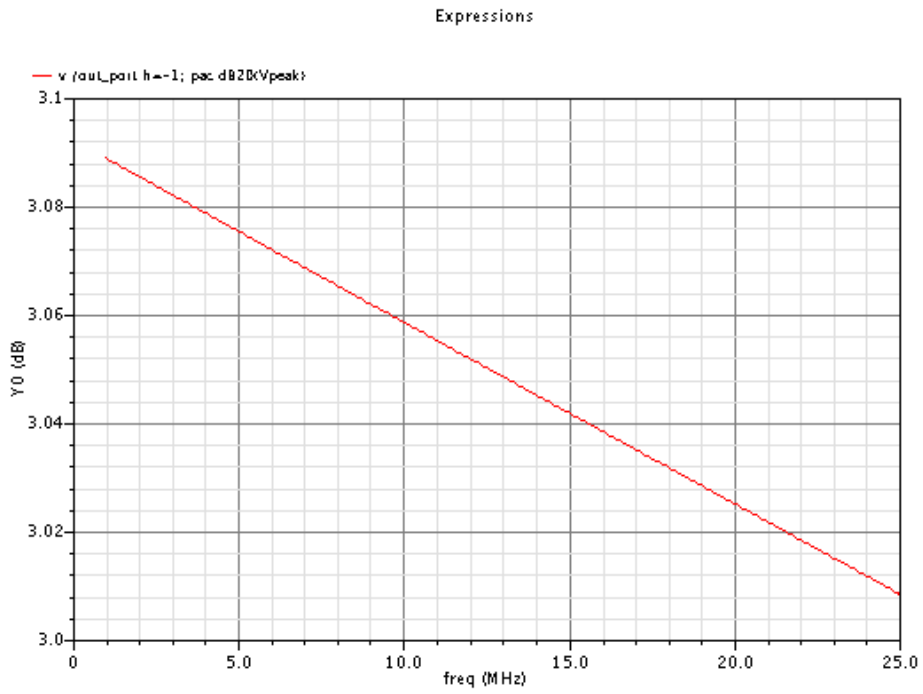


Fig. Power Gain of Mixer alone = ~ 3dB

ii) **LNA**

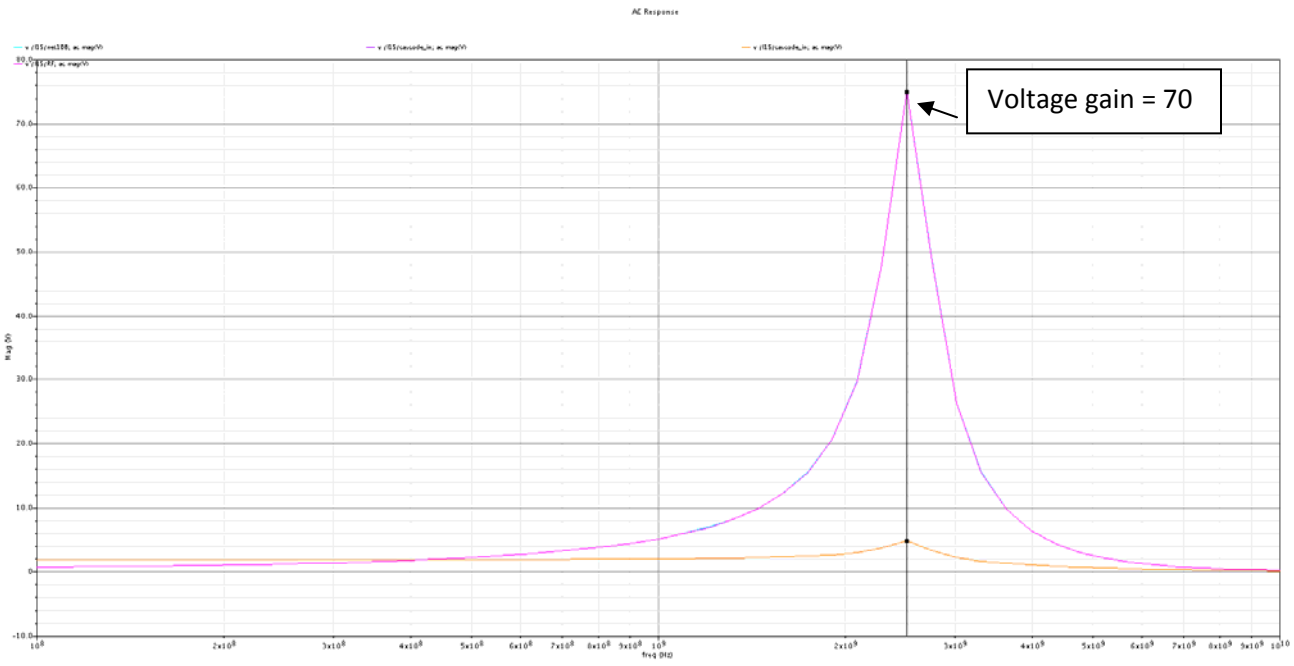


Fig. Voltage Gain of LNA Alone = ~ 70

2. **IIP3 of Mixer alone:** We simulated just the mixer part of our design on the given test bench and found its IIP3 = +4.5dBm. This means the LNA is really non linear and has degraded the final system's IIP3 down to -30 dbM. (Refer page 9)

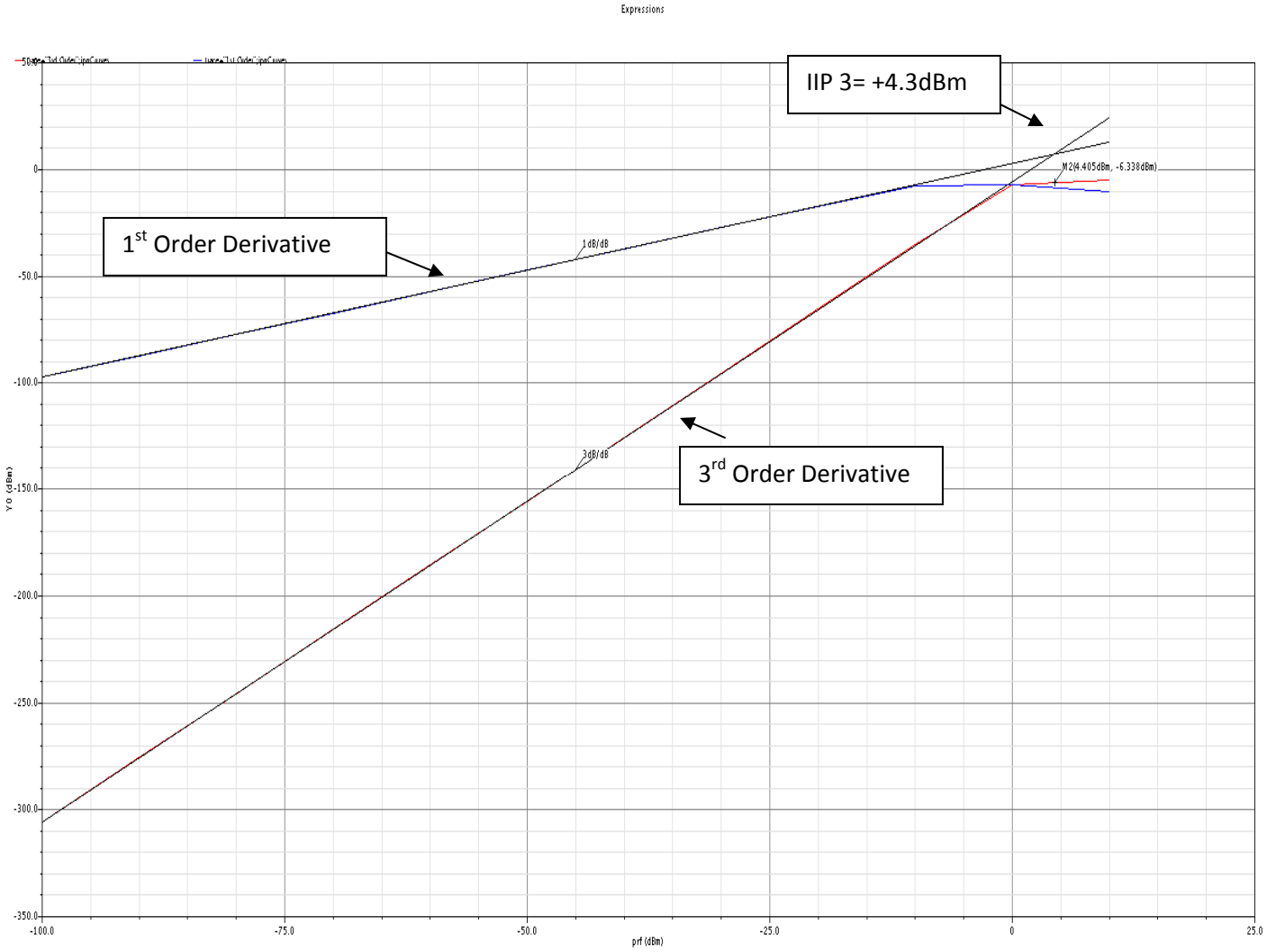


Fig. IIP3 of Mixer alone

3. Input Matching

We tried various ways to make sure we were implementing power matching between RF input and the LNA transistor. For this purpose we made some input impedance curves as follows: (See page 6)

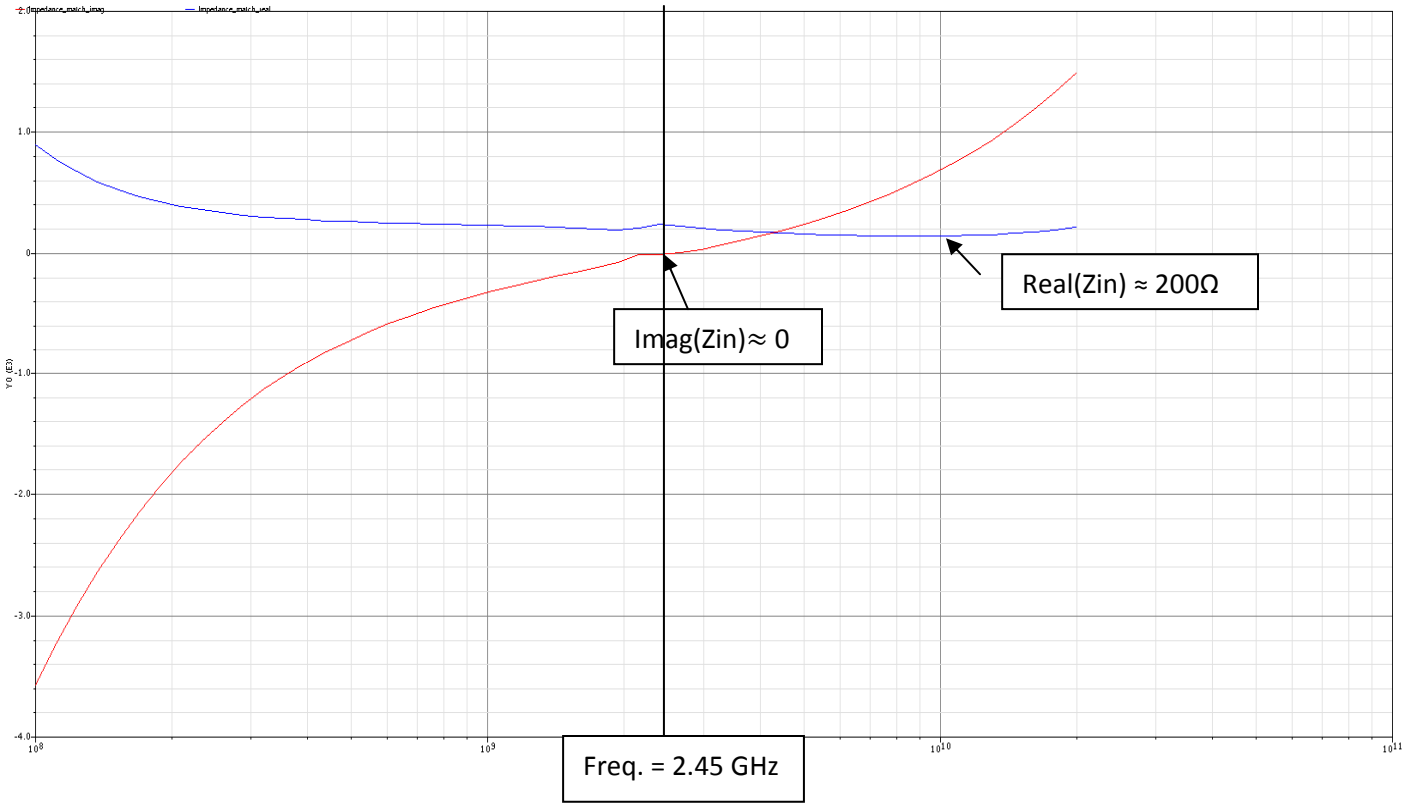


Fig. Input Impedance seen at RF input transistor of LNA

The real part of the resistance is seen as 200 Ohms due to 100 Ohms contribution from the source. The imaginary part of the impedance goes to zero in the required band, exactly as desired.

4. Linearity curves

The curves below show the **Gm** curves for the inductively degenerated Mixer transistor.

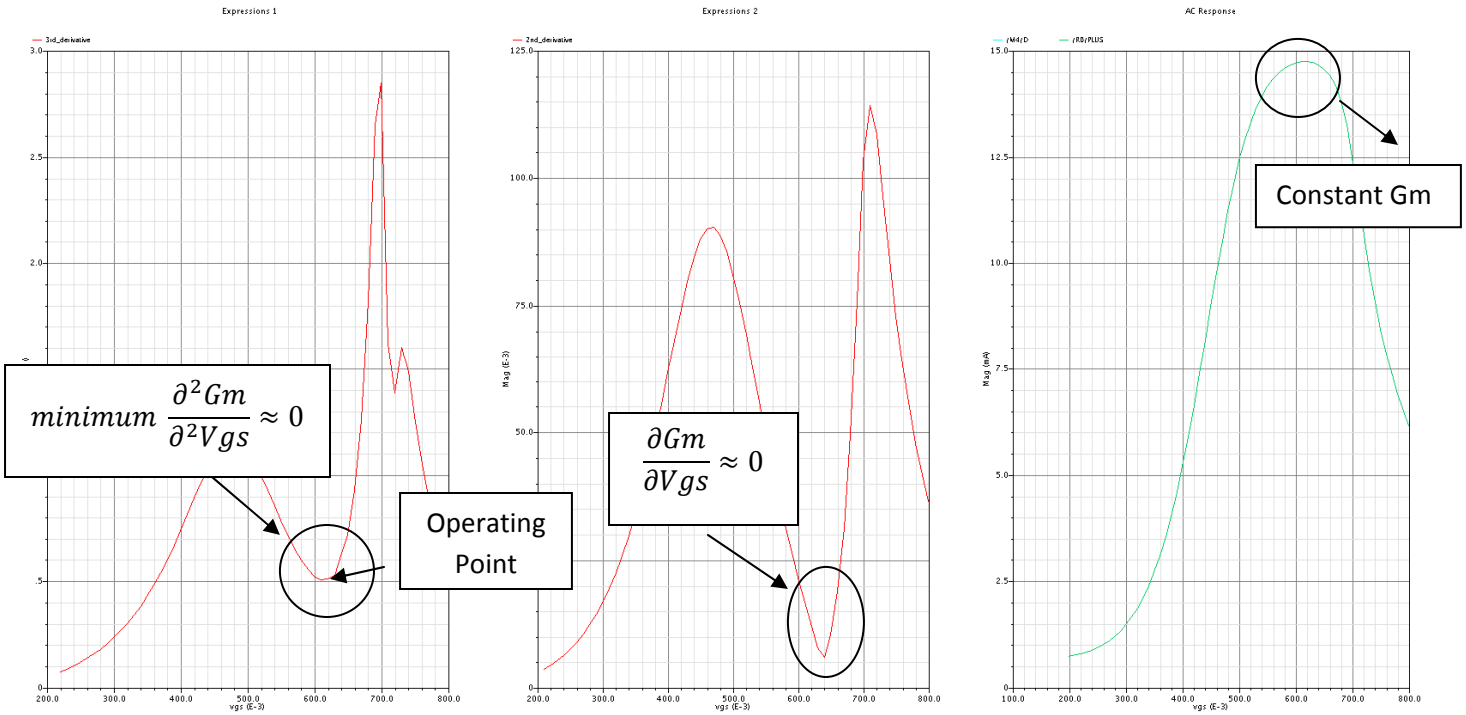


Fig. i) Second order derivative ii) First order derivative iii) Gm

We are operating at Vgs = 0.6V for the mixer as is shown to be the highest linearity point in above graphs. The inductance of 3.9nH (~4nH) for mixer degeneration has been selected by initially, doing the transient analysis of the LNA to determine the variation of RF signal to be ~ 100mV (peak-to-peak) on the input mixer RF transistor. This gave us an estimate of minimum degeneration inductance required on mixer design. The third derivative on the region of operation is minimum (as shown in figure) thus minimizing third order distortion.

5. Weak FeedForward Design – This is a schematic of the linearity improvement method we tried, which however did not give us any improvements. (See page 9)

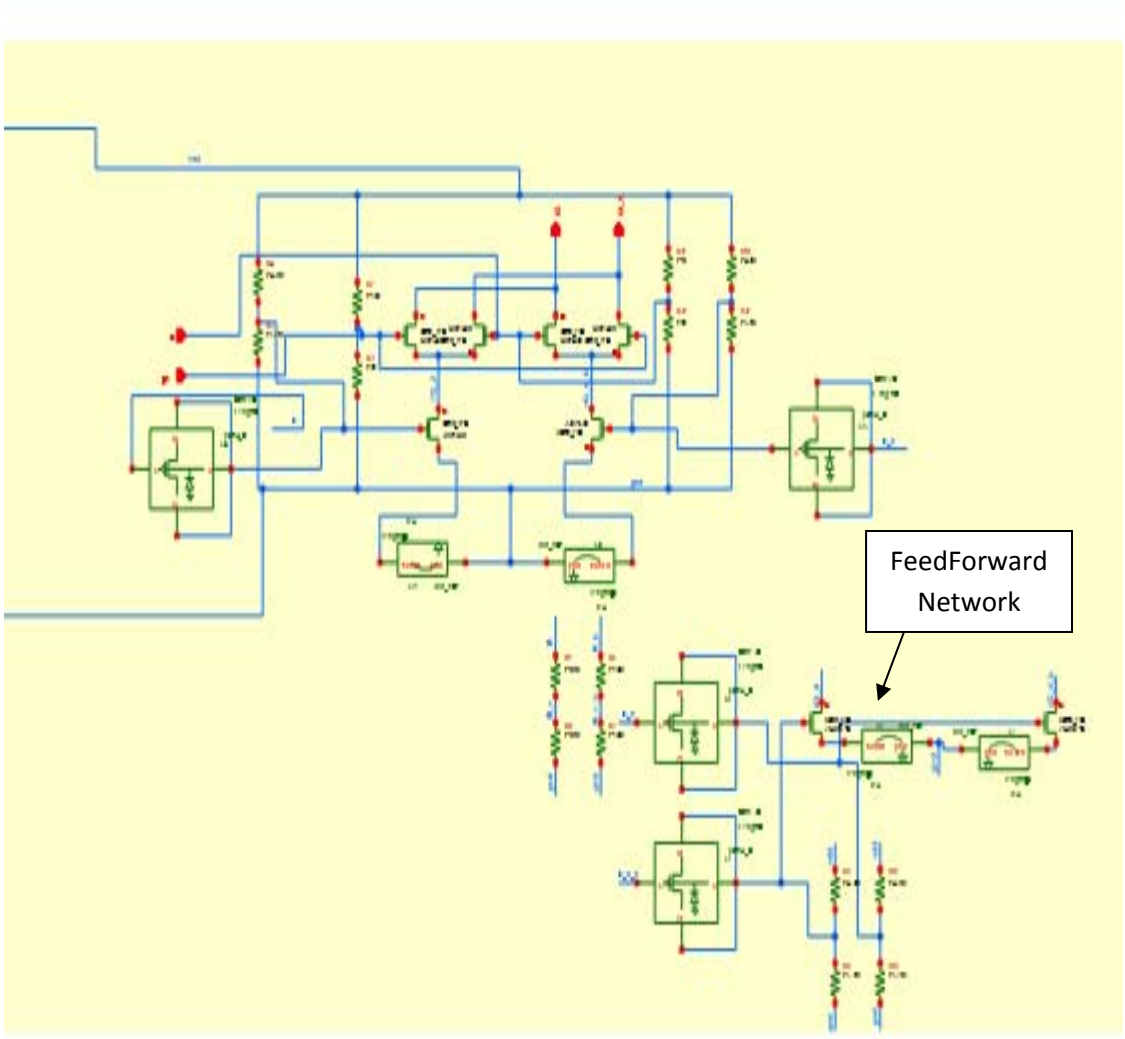
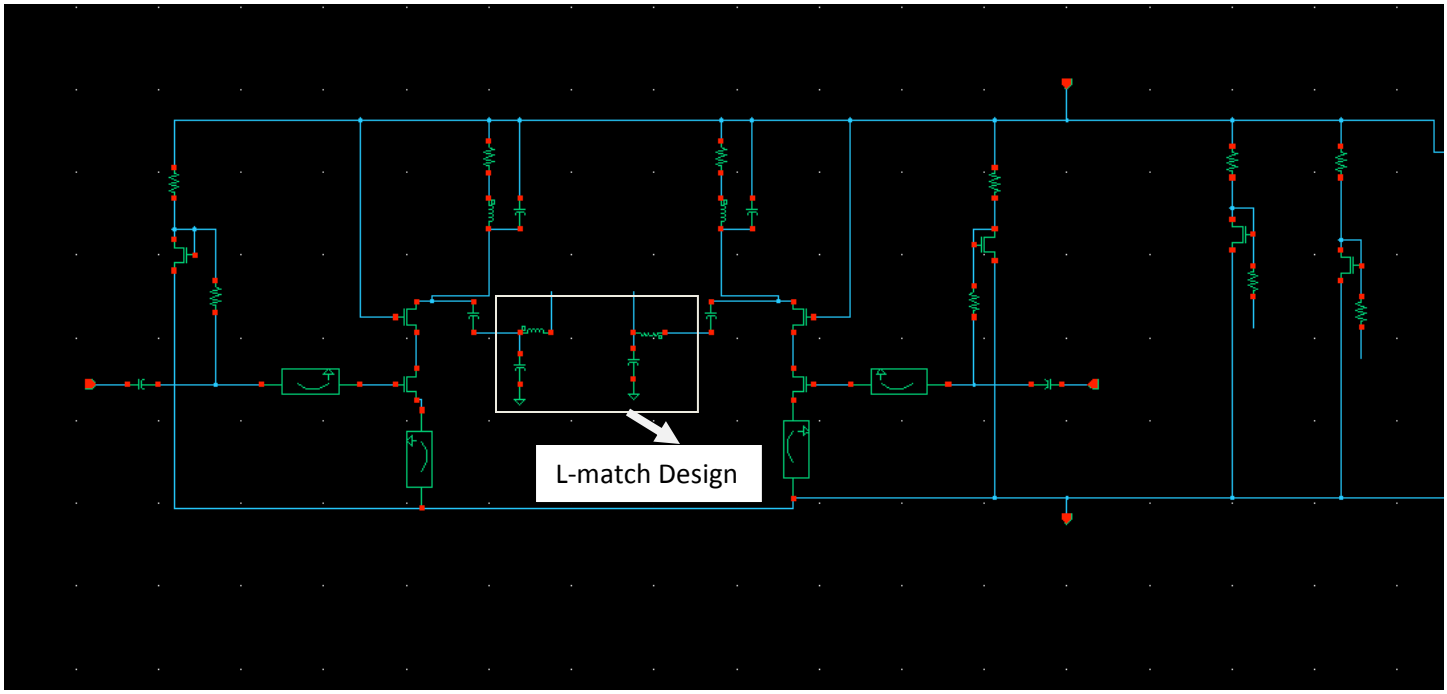


Fig. Weak Feed Forward Design for increasing linearity. N= 1.1, M = 1.33

6. L-Match



7. Highest Design Specs achieved: Below are gain and linearity curves of the two other designs we made. The one with high gain gave low linearity while one with high linearity gave a small gain.

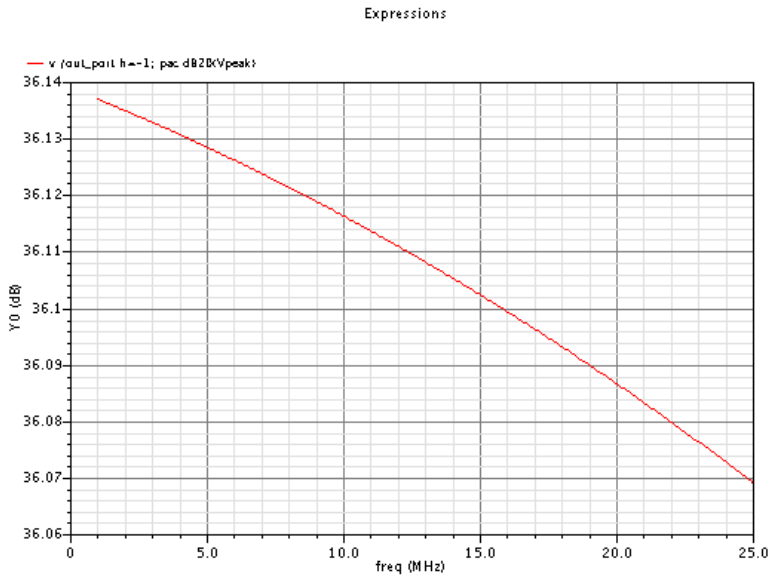


Fig. Highest Gain 36dB achieved at 2.45G by reducing inductance in source of mixer transistor to 1 nH from 4nH

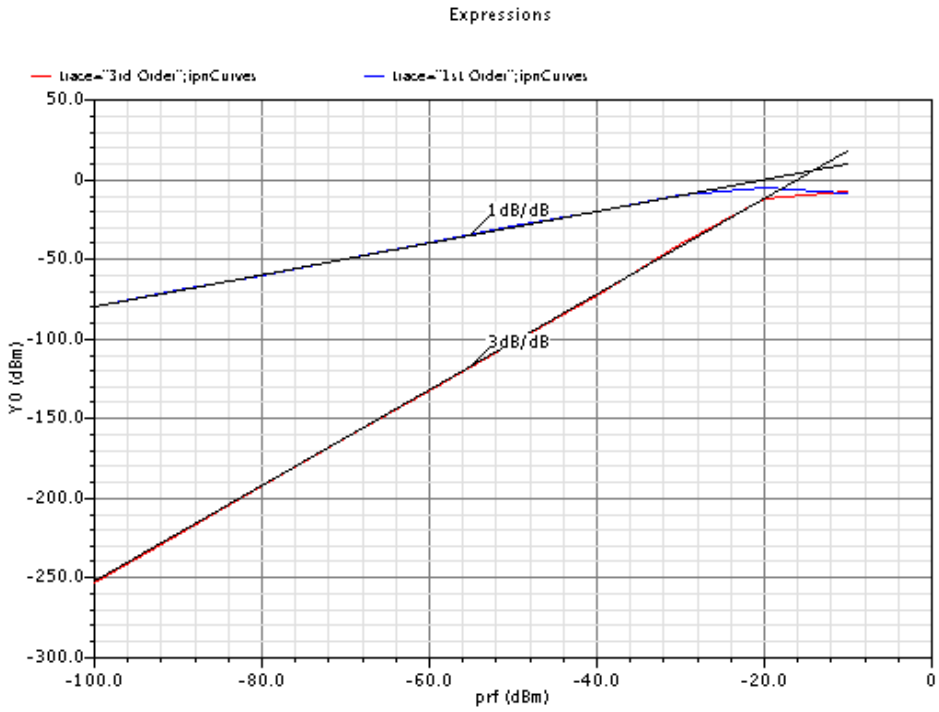


Fig. Highest Linearity -13dBm achieved at 2.45G by increasing inductance in source of mixer transistor from 4nH to 8nH

6. **MATLAB Script**

```
clc
clear all
%optimum_Rs=100;
cgd=300e-15;
Wo=2.45*2*pi*1e9;
%Lopt=2*optimum_Rs/Wt
Lreqd=(1/Wo^2/cgd)
% Given params
s=2e-6;
permeabilitymu=4*pi*1e-7;
eox=3.9*8.85*10^(-12);
skindepth=1.607e-6;
sigma=4*10^7;
t=1.2e-6;
tox=3.5e-6;
tmm=0.3e-6;
c1=1.27;
c3=0.18;
c2=2.07;
c4=0.13;
Rsmax=0;
%INDUCTANCE OF A SPIRAL INDUCTOR
% Supplied parameters
%N=7 FOR 10nH

for n=1:1:15
   %n
   for width=2e-6:1e-6:30e-6
      a=ceil((2*n*width - 2*(n-1)*s)*1e6)*1e-6;
      for Dout=a:10e-6:1500e-6
         for s=2e-6:0.1e-6:4e-6
            Din= Dout - 2*n*width - 2*(n-1)*s;
            Davg=(Din+Dout)/2;
            ro=(Dout-Din)/(Dout+Din);
            if ro>0
               l=width/2+4*n*(Dout-width) - (2*n-
1)^2*(s+width);
               Cp=n*width^2*eox/tmm;
               Rs= l/(width*sigma*skindepth*(1-exp(-
t/skindepth)));
               Cox=l*eox*(width/tox + 0.77 +1.07
*((width/tox)^0.25 +  (t/tox)^0.5));
               %log(c2/ro);
               if (log(c2/ro) > 0)

L=0.5*permeabilitymu*n*n*Davg*c1*(log(c2/ro) + c3*ro+
c4*ro^2);
                  if (abs(L-Lreqd)<1e-11)
                     Q=Wo*L/Rs;
                     if (Q>6 && Q<8)
                        if (Rs>Rsmax)
                           Coxopt=Cox;
                           Qopt=Q;
                           Rsmax=Rs;
                           Nopt=n;
                           Widthopt=width;
                           Doutopt=Dout;
                           Sopt=s;
                           Lvalue=L;
                        end
                     end
                  end
               end
            end
         end
      end
   end
end
Rsmax
Nopt
Widthopt
Doutopt
Lvalue
Lreqd
Sopt
Qopt
Coxopt
```