A 3.2GS/s 5-Bit Time-Interleaved Flash ADC in 0.18um CMOS Technology

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***Abstract*—A 3.2GS/s, 5-Bit time-interleaved, fully differential and calibration-free flash Analog-to-Digital (ADC) on 0.18um N-well CMOS process is designed and simulated. Each element of array of 8 A/D converters operates at 400MS/s and can sample up to 1.6GHz input signal. The achieved SNDR at Nyquist Rate (fs/2=200MHz) is 27.9dB and at maximum input rate (4*fs=1.6GHz) is 25.5dB .i.e. ENOB is 4.34 at 200MHz and 3.94 at 800MHz. The A/D converter occupies 287mW from a 1.8-V supply, achieving Figure of Merit, FOM of 1.79*10-18Js at 400MS/s. Static DNL error is determined to be 0.178 LSB.**

***Index Terms*—Flash A/D Converter, Reference Ladder, clocked Bootstrap switch.**

I. Introduction

ANALOG-to-Digital converter is one of the most important building blocks in current systems design ranging from radar & optical communication links operating at very high speed, to high precision sensors operating at very low frequencies. Flash ADCs are the fastest among all the ADC architecture family members because of least number of design stages present during data conversion.

High-data-rate applications such as optical communication links rely on high-speed ADCs with ~5 bit Resolution and high sampling rates (~1-5 GS/s). The time interleaved flash-ADC proposed herein is able to meet such specifications by burning low power and sampling Data in parallel.

Complete A/D Differential System has been implemented to increase the effective signal swing, reducing common mode noise and increasing the speed of T/H & comparator stage by reducing size of comparator and meeting σ_{DNL} specifications by increased input signal swing. Each A/D converter consists of Track-and-hold stage to sample the input wave; Comparator stage consisting of (2^5-1) comparators to compare input swing with reference signal swing; and Reference ladder to provide reference signal swing.

Each comparator in the A/D converter has been designed as a combination of clocked linear pre-amplifier, integrator and latch based amplifier to have desired high gain and high performance in terms of low metastability (see sec III). Using additional sampling capacitor has been avoided in the design, as to increase the sampling rate of the A/D converter and to reduce excessive loading of T/H stage; as having large sampling capacitor increases the time constant in tracking phase and results in limiting the speed & output swing of T/H circuit.

Clock bootstrapping has been implemented for the track-and-hold stage to have switch resistance and channel charge injection independent of the large input signal swing for the first order and hence, have lower distortion on the signal being sampled and have higher SNDR performance. Sampling frequency, f_s has been increased to improve the figure of merit (FOM) given by,

$$FOM = \frac{P}{f_s^{\,2}}$$

where, P is the power consumption of the design and f_s is the sampling frequency of the individual A/D converter (see Table1.). Power consumption has been reduced by designing completely dynamic comparator including the linear clocked pre-amplifier stage and minimizing any static power consumption in comparator stage. Reference ladder has been designed using resistive divider network and resistor value has been optimized to have good SNDR performance, reduced kickback effect with least static power consumption. Reasonable size of capacitors has been added in the reference nodes of the reference ladder to reduce kickback effect and high frequency distortion further, arising because of coupling of output signal with the input reference signal. The approach while designing the system has been to increase the sampling rate with reduced input signal swing and to minimize power to improve figure of merit (FOM).

Each of the stages of the S/D converter system design has been described in the section II. Section II. contains the detailed explanation of design approach being followed. Section III discusses the simulation results being obtained. Section IV describes the conclusion and section V points out the future work that can be implemented to enhance the performance of the A/D Converter.

II. Circuit Implementation

This section describes about the design strategy being implemented for the complete system. System has been divided into 3 stages – Reference Ladder, Track-and-Hold (T/H) and Differential Comparator. Each is of the blocks is discussed in following section. The block diagram for the A/D converter is as shown below:

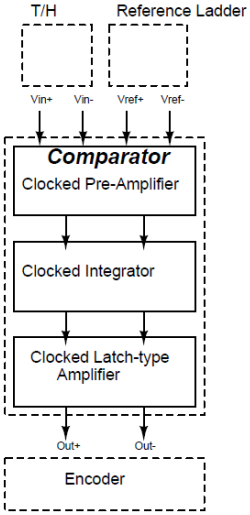

Fig1. System Block Diagram

1. *Reference Ladder*

Resistive reference ladder has been designed to maintain linearly varying reference voltage swing on each of the 2^5-1 comparators. Any non-linearity on the reference voltage results in improper comparison between input and reference signal of comparator and hence lowering the SNDR performance of the A/D converter. To minimize static power consumption on the reference ladder, large resistors are required in designing reference voltages for the comparators. However, larger the value of the resistor more is the coupling and kickback noise on the input reference signal from the changing output signal while comparing the input with reference. This kickback noise may result in changing reference signal and hence results in improper comparison with the input signal and reduces the SNDR performance of the design. Hence, this tradeoff between the static power consumption and kickback noise optimizes the resistor being used in the design. Optimum total resistance used in each of the two resistive ladders is **R_{total} ~ 2.24kΩ**

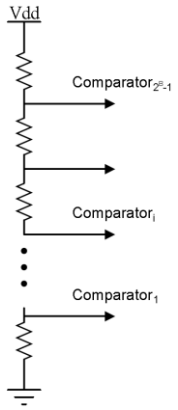

Fig2. Reference Ladder Circuit

Bypass capacitors (~400fF) has been added to each of the nodes of the resistive ladder to reduce kickback noise and reduce high frequency coupling between reference and output. This has resulted in improving the SNDR from 27.5dB@f_s/2=200MHz to 27.9dB by including bypass capacitor.

2. *Clock Bootstrapped Track and Hold*

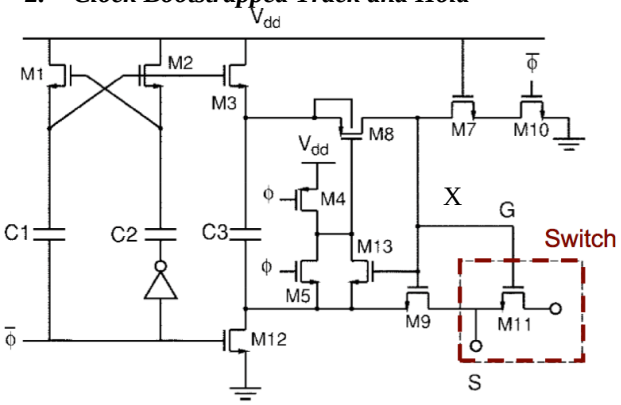

Fig3. Clock bootstrapped T/H Circuit

A clock bootstrapped T/H circuit has been utilized in this design in order to maintain a fairly low and constant 'ON' resistance (M11, Fig3.) during track phase, as clock bootstrapped circuit maintains Vgs_{M11}~Vdd irrespective of the input signal. The 'ON' resistance of the NMOS switch is chosen such that the 50Ω source impedance is large as compared to the switch and switch doesn't result in attenuating signal by significant drop across its terminal. As a result, the appropriate size of the NMOS switch was determined by simulating the on resistance of an NMOS switch vs. device width while holding Vgs ~ Vdd. This gave an estimate of keeping size of switch transistor (M11) to be greater than 40µm. However, as the size of M11 is increased, it results in increasing the parasitic and Cgs_{M11} capacitors of the transistor which results in excessive clock feedthrough as parasitic capacitors including Cgs_{M11} of switch transistor comes in parallel to the sampling gate capacitor of the (2^5-1) comparators. This resulted in drop in the common mode supply for the comparator during the comparison phase (see Fig5.). In addition, since this device dominates the contribution of parasitic capacitance from the gate, a large device would be more difficult to switch on and off. A modest width of 60µm was chosen. Design considerations for the rest of the components of the Track-and-Hold design are as follow:

C3: Size of C3 capacitor needs to be large enough so that the C3*Vdd charge across its two terminals can be directly transferred to the Gate and source terminals of the switch transistor, M11 without resulting in drop across its terminal while sharing charge with the Cgs and parasitic capacitors of the M11, M13, M7 & M9 (see Fig5.). To account for charge sharing, size of C3 has been kept ~25x size of node capacitor, C_X.

Total capacitor across node X,
Cx = Cp + Cgs11 + Cgs13 + Cgs7 + Cgs8 + Cgs9 ~ 300fF

Nominal size of C3 chosen to be = 8pF
Charge Reduction = Cx/(C3+Cx) ~ 3.6%

Transistor Sizing: M1, M2, M3 and M12 have been sized to

ensure that the transistors are strong enough to charge or discharge respective nodes to vdd and gnd during the track or hold phase. Nominal size of W3, W12 = 30µm and W1, W2 = 40µm have been selected based upon these considerations. These values resulted in roughly equivalent time constants to balance the timing of the track and hold phases.

Inverter: Inverter characteristics have been studied and rise and fall time of the inverter has been observed. Through simulations it was observed that for the given technology Wp/Wn ratio needs to be maintained ~ 2.2X for the same rise and fall time. Also, since the inverter is driving load, C1 (~0.5pF) it was sized to ~1/4X (for optimum output rise and fall time while driving load) i.e. Wn=40µm and Wp=88µm.

M8 is a switch resistor and has C_X as the load capacitor. Since, Vdd across C3 charges node C_X, size of M8 can be determined by computing the time constant, $\tau = Ron_{M8} * C_X$ and minimizing it. However, too large size of M8 results in large parasitic at node X and results in increasing Cx and reducing time constant, resulting more clock feedthrough during comparison phase. 'ON' resistance of M8 has been determined similar to M11 and has been sized to, W_{M8}~ 40µm.

M7 and M10 acts as resistive load while discharging gate node of switch transistor M11 to ground in hold phase and hence has been sized to ~30um to maintain low resistance without contributing large parasitic on X.

M4, M5 has been sized (1/4X of W_{M8}) as this inverter has Cgs of M8 as load and has been optimized in similar fashion as the inverter discussed above. W_{M4}=20µm and W_{M5}=10µm.

Capacitors: Capacitors, C1 & C2: Capacitor, C1 needs to be large enough to put 2*Vdd on the gate node of M3. It has been designed in similar fashion as C3 has been sized. However, total gate and parasitic capacitors seen by C1 is lesser (~1/8X as compared to Cx) and hence, C1 ~ 0.5pF. C2 has been sized similarly and ~ 0.5pF.

Device M13 ensures that Vgs8 does not exceed and can be sized to ~ 10um ensuring that the driving strength of M13 is not too low and does not contribute to parasitic.

3. *Differential Comparator*

5-bit flash ADC requires 2^5-1 instantaneous comparisons using 2^5-1 comparators in the design which results in heavily loading the Track-and-Hold (T/H) stage and increasing the effective capacitance while tracking data. Since, the total gate capacitance of the comparator stage in the design are large (~1-2pF) due to offset requirements (explained in the following section), using additional sampling capacitors has been avoided. Total gate capacitance of the comparators has been utilized as the sampling capacitor. Since, the input sampled signal has low swing the Comparator is required to have very large gain so that it switches to either greater than 0.9*Vdd or less than 0.1*Vdd in the given hold clock cycle (2/fs).

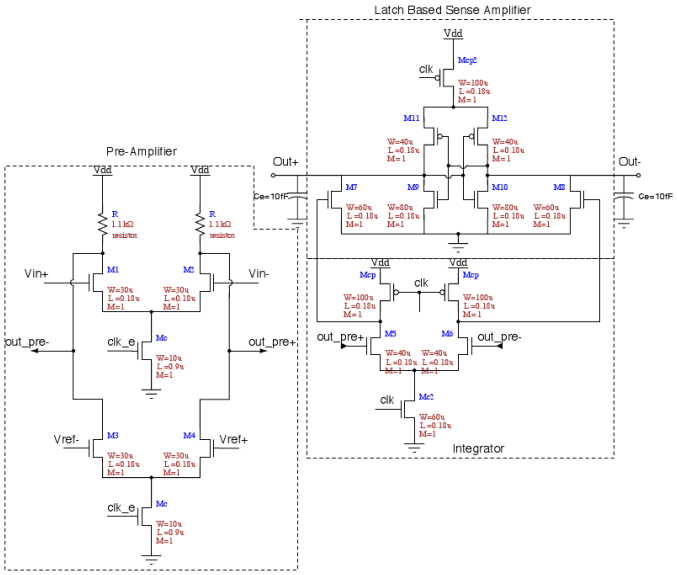

Fig4. Comparator Architecture (See Appendix for larger image)

To achieve high performance in terms of speed and considering metastability and taking loading T/H stage into effect, each comparator in the A/D converter has been designed as a combination of linear pre-amplifier; integrator and latch based amplifier (see Fig4.). However, all the three sub-stages in the comparator design have been clocked to minimize static power consumption in the design.

Offset Specifications: Since, the offset specifications are known; it gives us a ballpark figure of sizing of the input transistors of the comparator stage. Now, the σ_{os} is given by,

$$\sigma_{os} = \frac{\sigma_{DNL} \times LSB}{\sqrt{2}} \quad where \;\; LSB = \frac{2V_{FS}}{2^B - 1}$$

Through literature survey, we started with the idea of using dynamic double-tail latch based sense amplifier to have high performance design. Since, the approach while designing the system is to obtain high sampling frequency, the input signal swing could not be very large as track-and-hold stage starts limiting the performance for high input signal swing at very high frequencies because of large static and dynamic residue signal. As a result, the input signal swing was assumed to be V_{fs} ~ 300mV @ fs=400MHz. While using the value of V_{fs} it gives the estimate of the transistor widths, conservatively assuming that threshold voltage mismatch from subsequent stages after the first stage directly add to the input (even though they will be divided by the gain of the stage and assuming that the gain of the 1st stage is ~ 1-2).

$$\sigma_{os} = 2.7mV \; and$$
$$\sigma_{os}{}^2 = 3\sigma_{Vt}{}^2$$

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}} \; with \; A_{Vt} = 4 \; mV \cdot um, L = 0.18 \; um$$

$$W_{min} = 36.6 \; um$$

Clearly, this indicates that the sizes of the input transistors mainly determine the offset voltage requirements of the comparator or the DNL specs for the system. Also, this analysis has been simplified by considering the effect of only the driving transistors mismatch. Hence, the input stage transistor sizes need to be large enough ~ 30-40µm.

Initially, only integrator was preceding latch based amplifier stage. However, because of dynamic nature of the integrator stage whenever system changed mode from Track stage to hold stage; as clock signal (clk) goes 'High', it results in drastically increasing the Cgs capacitors(M5-M6, Fig4.) of the input transistors of the comparator integrator stage. This increase in Cgs capacitors is because of change of mode of operation of the Transistors (M5-M6) since as clock goes 'High' it goes from 'off' state of infinite source degeneration to 'ON' state with no source degeneration (see Fig4.). Also, because of the offset requirements, size of the input transistors could not be reduced to minimize the dynamic effect of changing gate capacitance. This drastic increase in gate capacitor during hold stage results in charge sharing of the the sampled data and reduces the input signal swing on the comparator (see Fig5.).

To minimize reduction in the sampled signal and preserve the input signal swing, Preamplifier stage has been included ahead of integrator stage. However, to reduce the power consumption pre-amplifier stage has been clocked. But, the size of input transistors need to sized large enough as discussed above, to meet the DNL specs of the system. To mitigate the effect of the dynamic switching and changing gate capacitance, clock signal applied to pre-amplifier starts early (~ 200ps) before track phase goes 'OFF' completely. This results in burning static power to some extent (~10%) but, it helps in maintaining constant Cgs on the input nodes when the system switches from Track-to-Hold phase. It should also be noted that during this time interval though pre-amplifier starts amplifying the signal (even before track phase goes 'OFF') the comparator does not start comparing data as the clock input input to the comparator is still 'LOW'. Also, this method (early clock signal) could not have been applied directly to the integrator stage as the Cgd coupling from output node is much more as compared to resistive pre-amplifier and would have resulted in droop in the input signal and improper comparison even after burning static power. This result can be seen in Fig5 & Fig6. below:

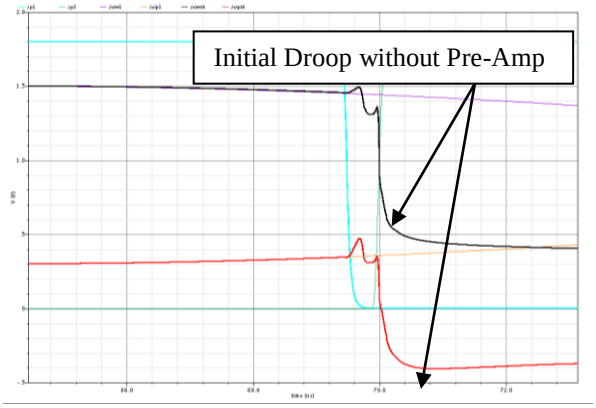

Fig. 5. Clock bootstrapped T/H Circuit

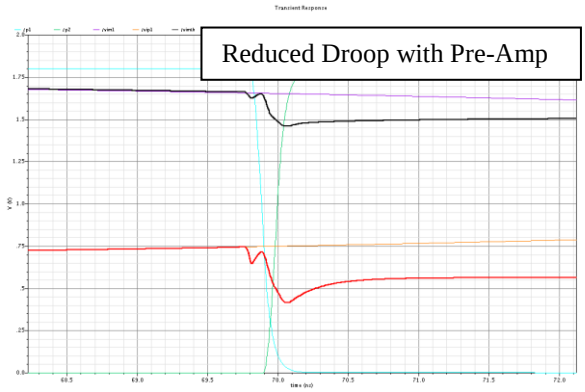

Fig. 6. Clock bootstrapped T/H Circuit

The design considerations for each of the sub-stages for the comparator are described in the following section.

3.1 Pre-Amplification stage

Differential dynamic resistive load amplifier has been designed as the pre-amplification stage (Fig4.). Input transistor sizing of the pre-amplifier has been designed mainly by considering the DNL specs and σ_{os} requirements for the comparator as discussed in the previous section. Hence, the input transistors M1-M4 have been sized as, W ~ 30µm. Size of clock transistor has been selected to ensure deep triode operation of the transistor during 'ON' phase. Since these transistors are clocked to the supply voltage, the lengths had to be increased in order to pull less current through the differential pairs. Load Resistor value has been determined to maintain voltage gain of more than 1 (~2.5).

3.2 Integration and Latch type Sense Amplifier Stage

The latch and integrator stage has been sized in order to improve individual figure of merit, FOM. Analysis of this structure can be simplified by diving the stages and considering individually, with the start of the latching phase occurring at the end of the integrating phase. In actuality, this is not the case since latching is happening during integration, but the assumption provides valid estimates. If the latch is assumed to be initially operating where all of the transistors are in the active region, an expression can be written for the differential output of the latch, V_{od}, as a function of a step

input to the latch, V_{id} as follows:

$$V_{od}(t) = V_{id} \times \frac{g_{m7}}{G_m - \frac{1}{R_a}} \times \left(e^{\left(\frac{G_m - \frac{1}{R_a}}{C_L}\right)t} - 1 \right)$$

$$G_m = g_{m9} + g_{m11}$$
$$C_L = C_{gs9} + C_{gs11} + 4C_{gd9} + 4C_{gd11}$$
$$R_a = r_7 || r_9 || r_{11}$$

$$\tau = \left(\frac{C_L}{G_m - \frac{1}{R_a}} \right)$$

It is clear from this expression that a small value of τ is desired in order to meet the metastability specifications. The latch was optimized in such a way as to maximize τ while burning as little power as possible. A defined figure of merit is given as:

$$FOM = I_b \times \tau$$

In Fig7. & Fig8., the individual FOM expression for the latch is plotted against the NMOS and PMOS (M9-M11) latch widths for Vout=200mV, 500mV, and 800mV (different bias points). An optimal FOM is achieved for Wp=40µm and Wn=80µm. It was not evident until later in the design that too much emphasis was actually given to (gm/C) in the FOM of the latch transistors. The metastability specification was met by a healthy margin (as shown above) and the speed of the latches actually do not end up dictating the ultimate operating frequency of the ADC since the bottleneck occurs from the input capacitance of the preamplifier stage, in conjunction with the source impedance. M7 and M8 were sized approximately the same as M9 and M10 to ensure an adequate static gain term in the latch. This analysis is clearly in terms with the theoretical approach, as large size of pmos does not helps with increasing latching speed but rather increases the load capacitance and hence, have smaller size as compared to the respective nmos transistors.

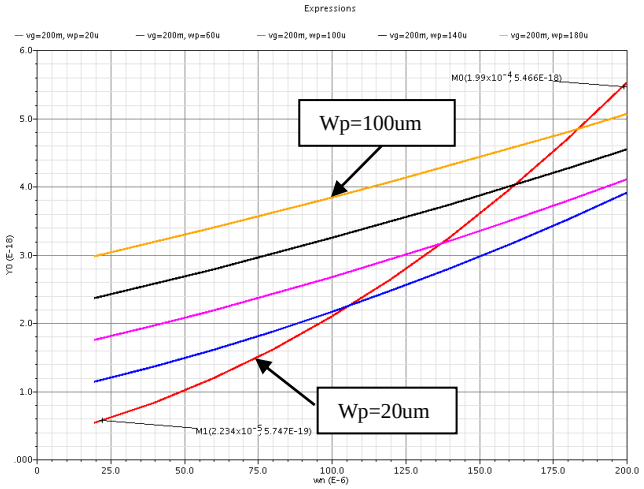

Fig. 7. FOM vs NMOS Latch Widths with a static gate bias of 200mV for different PMOS Latch Widths

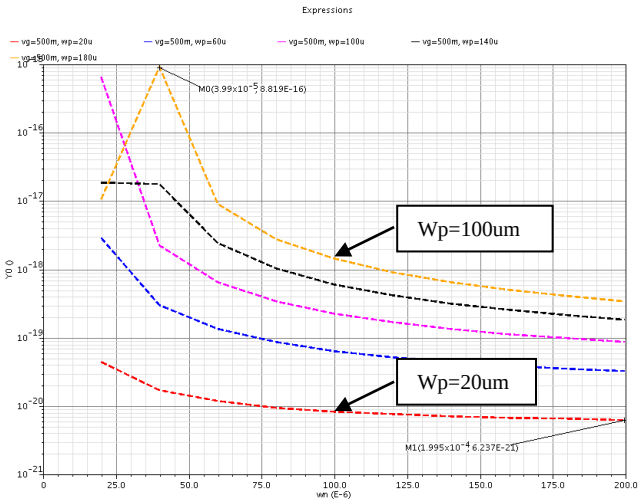

Fig 8. FOM vs NMOS Latch Widths with a static gate bias of 500mV for different PMOS Latch Widths

The integrating transistors M5 and M6 were sized according to the DNL specification. Since relatively small devices were intended to be used at the preamplifier stage, these transistors were also kept relatively small (W=60µm), since the contribution from offset is divided by the gain of the preamplifier stage. During the initial design that had not included the preamplifier stage, simulations showed that the comparator was giving incorrect comparisons at a low SNDR of 26dB. This was the result of sizing these devices too large and pulling too little current through them, resulting in a low ft frequency. Since the gain of the integration stage is (t*gm/C), an insufficient voltage differential was being developed at the output of the integrator.

III. Simulations and Results

The complete system has been analyzed individually and combined together to analyze the overall performance of the complete A/D converter system. Table1. below shows the achieved specifications and results of the design. Since, we had the choice of following two approaches with large signal swing & low sampling frequency or low signal swing with large sampling frequency; we designed for two approaches and have compared their performances as shown below (Table1). Design1 is the main focus in this report as it minimizes the figure of Merit, FOM and hence, has performance. The approach taken for Design 2 was similar for Design 1, but 20µm width sizes were used for the Pre-Amplifier transistors M3 & M4.

Specification	Design 1	Design 2
Process	0.18µm CMOS	0.18µm CMOS
Sampling Frequency, fs	400 MHz	333 MHz
Resolution	5 bit	5 bit
Supply Voltage	1.8 V	1.8 V
Differential Input Swing	+/- 350 mV	+/- 700 mV

Peak SNDR	@fs/2	27.9dB	28.1dB
	@4*fs	25.5dB	23.5dB
ENOB	@fs/2	4.34 bits	4.38 bits
	@4*fs	3.94 bits	3.61 bits
DNL		0.178 LSB	0.2 LSB
Metastability Rate		$5.2x10^{-19}$	$4.3x10^{-8}$
Power		287.44mW	322.3mW
FOM		**$1.79 * 10^{-18}$ Js**	$2.9 * 10^{-18}$ Js

Power	**Design 1**	**Design 2**
Comparator + Bias	128.96mA * 1.8V=232.12 mW	143.02mA * 1.8V=257.4 mW
Clock	29.79mA * 1.8V=53.62 mW	35.98mA * 1.8V=71.244 mW
Reference Ladder	1.7 mW	1.7 mW
Total Power	**287.44 mW**	328.7 mW

Table. 1. Achieved Specifications

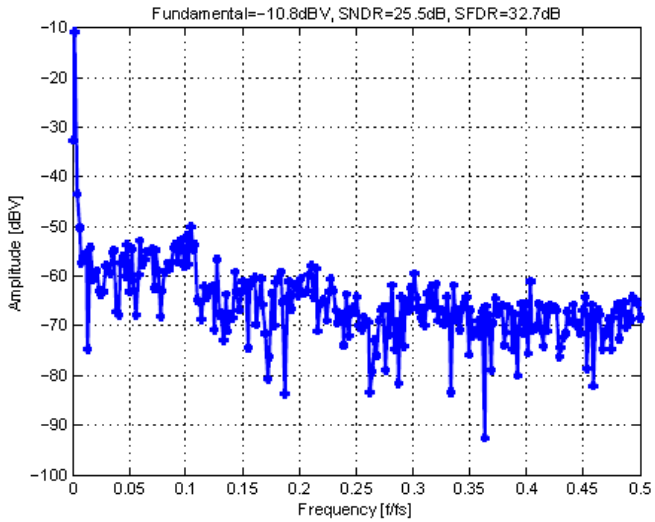

Fig 9. 4*f_s SNDR Plot 512 Point FFT

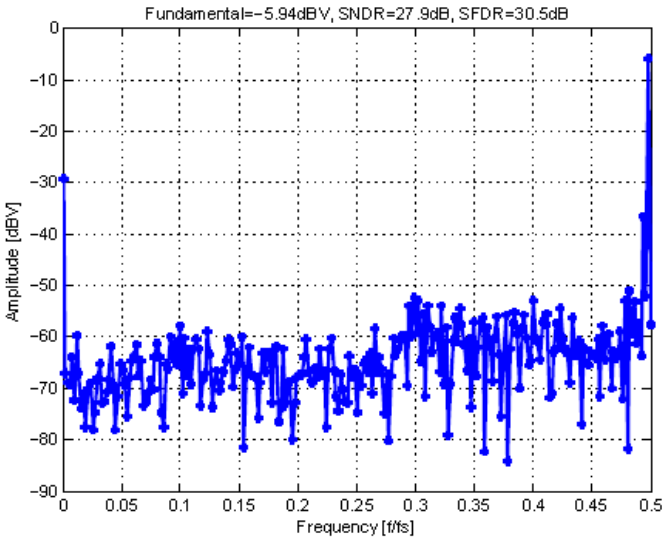

Fig 10. f_s/2 SNDR Plot 512 Point FFT

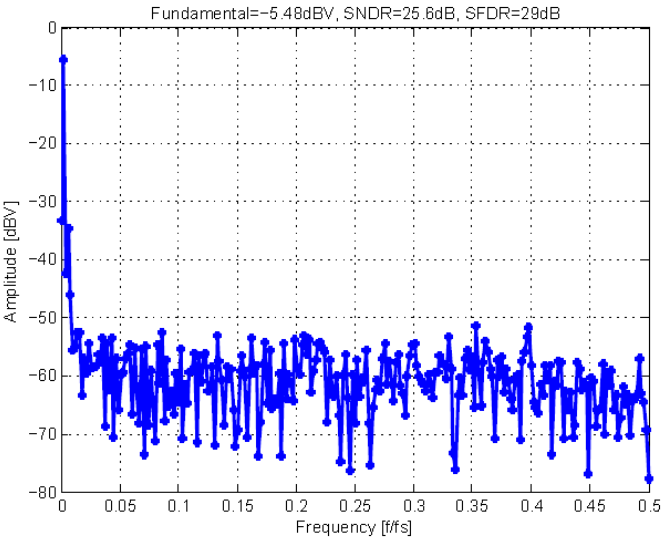

Fig 11. (1/512) * f_s (fin~780kHz) SNDR Plot 256 Point FFT

Monte Carlo Simulations for offset showed an achieved σ_{os} = 2.15mV as shown in the figure below:

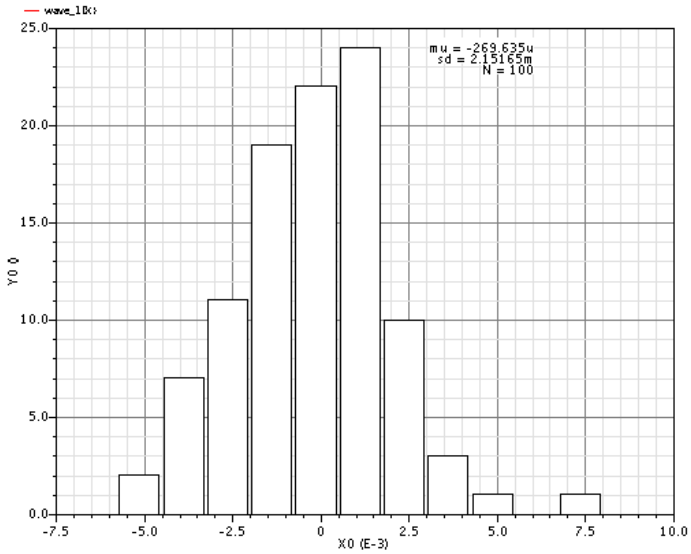

Fig. 12. Monte Carlo Run for Comparator Offset

Metastability Calculation

$$P(error) = \frac{1}{A_v}\frac{V_{DD}}{LSB}e^{\frac{-T_{max}}{\tau}}$$

$$T_{max} = 39.86ns - 38.86ns = .97ns$$
$$v_{com} = .6837V, v_1 = .7721V - v_{com} = .0884V, V1 = 0.7721V$$
$$v_2 = e \cdot v_1 = .2403V\ , V2 = v_2 + v_{com} = 0.924V$$
$$t_2\ @\ V2 = 38.884ns, \qquad t_1\ @\ V1 = 38.863ns$$
$$\tau = t_2 - t_1 = 2.078 \times 10^{-11}\ \text{s}$$
$$A_v = \frac{.5367V - .4482V}{.04V} = 2.21$$
$$LSB = \frac{.26V}{2^5 - 1} = 8.387mV$$

$$\underline{P(error) = 5.18 \times 10^{-19}}$$

Note: Refer to the Appendix for the extraction of τ and A_v

IV. Conclusion

The chosen architecture in this design allowed for the operation of a 5-bit Flash ADC with the ability to run at input frequency of $4*f_s$ i.e. upto 1.6GHz. The SNDR degraded at the $4*f_s$ frequency due to both the static and transient error terms from the T/H circuit formed by the time constant of the source/switch resistance and the input capacitance to the Flash ADC. In order to minimize the capacitance, sizing the preamplifier transistors small was crucial to maximizing the operating frequency. There was a bit of margin on the DNL specification, so this approach worked rather well in this design. Furthermore, SNDR was improved by using a bootstrapping T/H stage that minimized the on resistance of the switch. All of the comparator stages were designed in such a way as to minimize static current draw by dynamically clocking the amplifier/latch stages. Overall, this design strategy helped to minimize the FOM number.

V. **Future work**

There are certain areas in this design that can be better optimized to achieve a better FOM. When choosing the latch sizes initially, these devices were sized a bit too large since too much weight was given to maximizing the operating speed of the latch. These devices can most likely be scaled down in size to draw less power from the supply during dynamic switching.

Another potential design improvement could be the removal of the integrating stage since in this particular design there was quite a bit of gain. This would also reduce power consumption.

Averaging was not used in the preamplifier stage, but this could potentially allow for even smaller device size that could push up the $4*f_s$ frequency, since this would reduce the input referred offset of the comparator.

In practice, this circuit would potentially have some issues with common mode variations of the input signal since the common mode rejection of the preamplifier stage was not optimized.

References

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APPENDIX

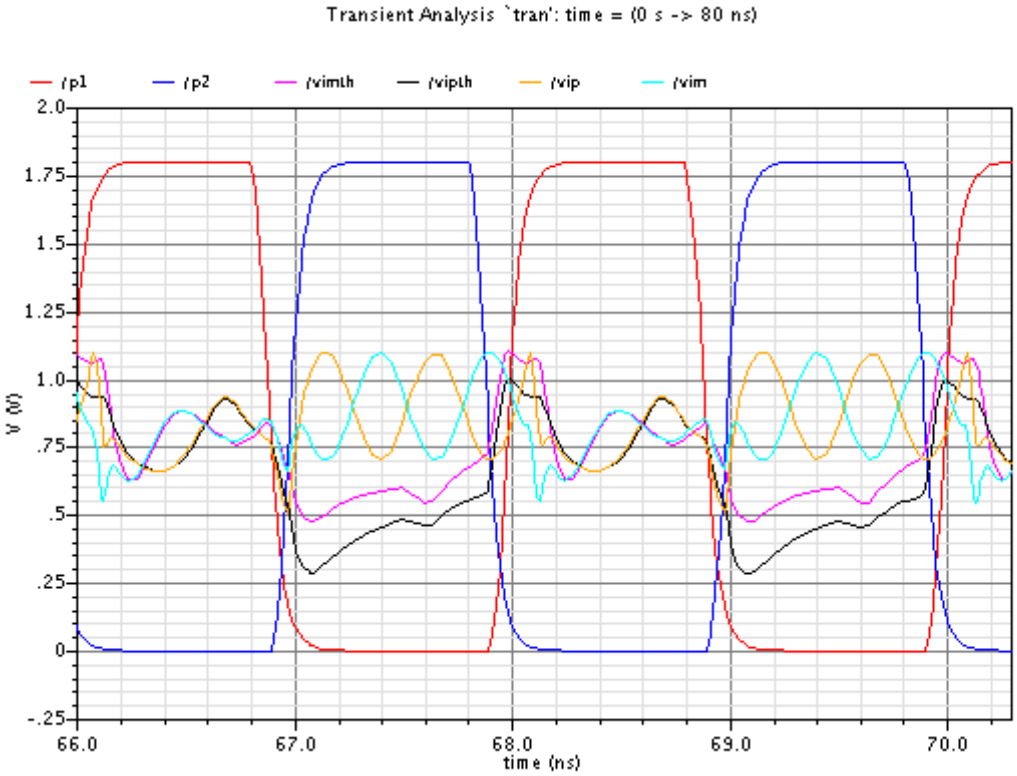

Fig. A1. $4*f_s$ track mode errors

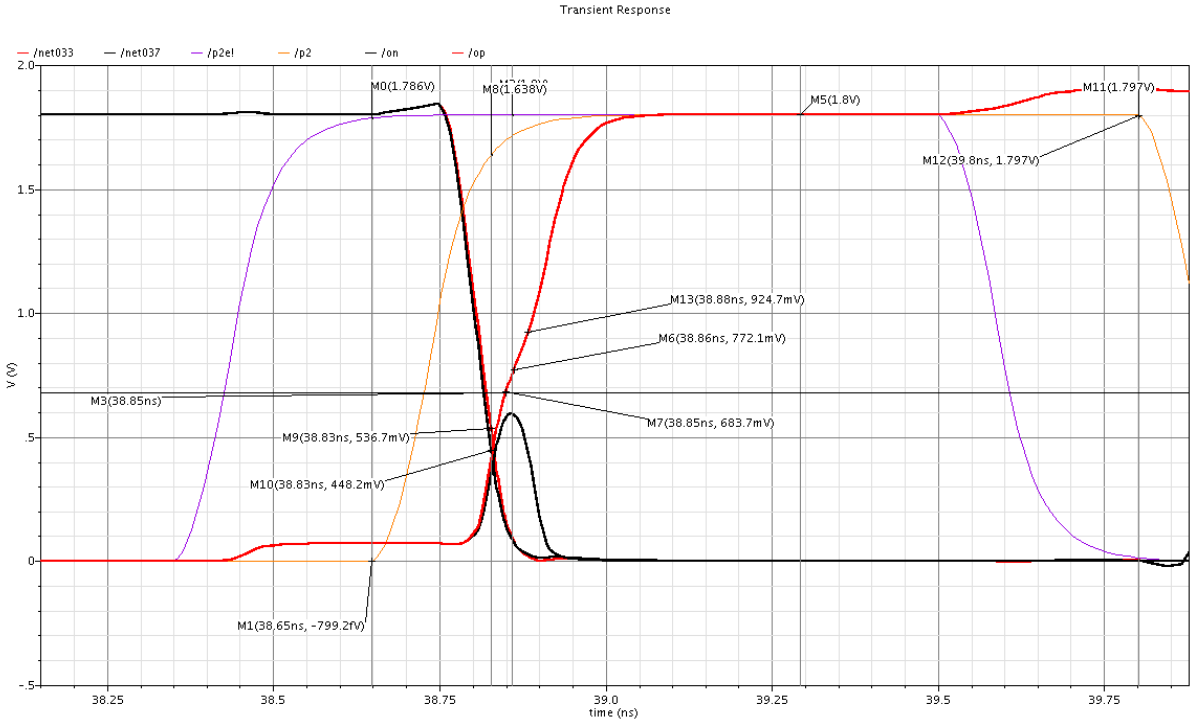

Fig. A2. Metastability Extraction Transient Plot

Parameter	Values
M1	W_{M1} = 40µm
M2	W_{M2} = 40µm
M3	W_{M3} = 30µm
M4	W_{M4} = 20µm
M5	W_{M5} = 10µm
M7	W_{M7} = 30µm
M8	W_{M8} = 40µm
M9	W_{M9} = 60µm
M10	W_{M10} = 30µm
M11	W_{M11} = 60µm
M12	W_{M12} = 30µm
M13	W_{M13} = 10µm
C1	C_1 = 8pF
C2	C_2 = 500fF
C3	C_3 = 500fF
Inverter	NMOS: W/L = 40µm/1.8µm
	PMOS W/L = 88µm/1.8µm

Table. A1. Device Sizes for Clock Bootstrap Circuit

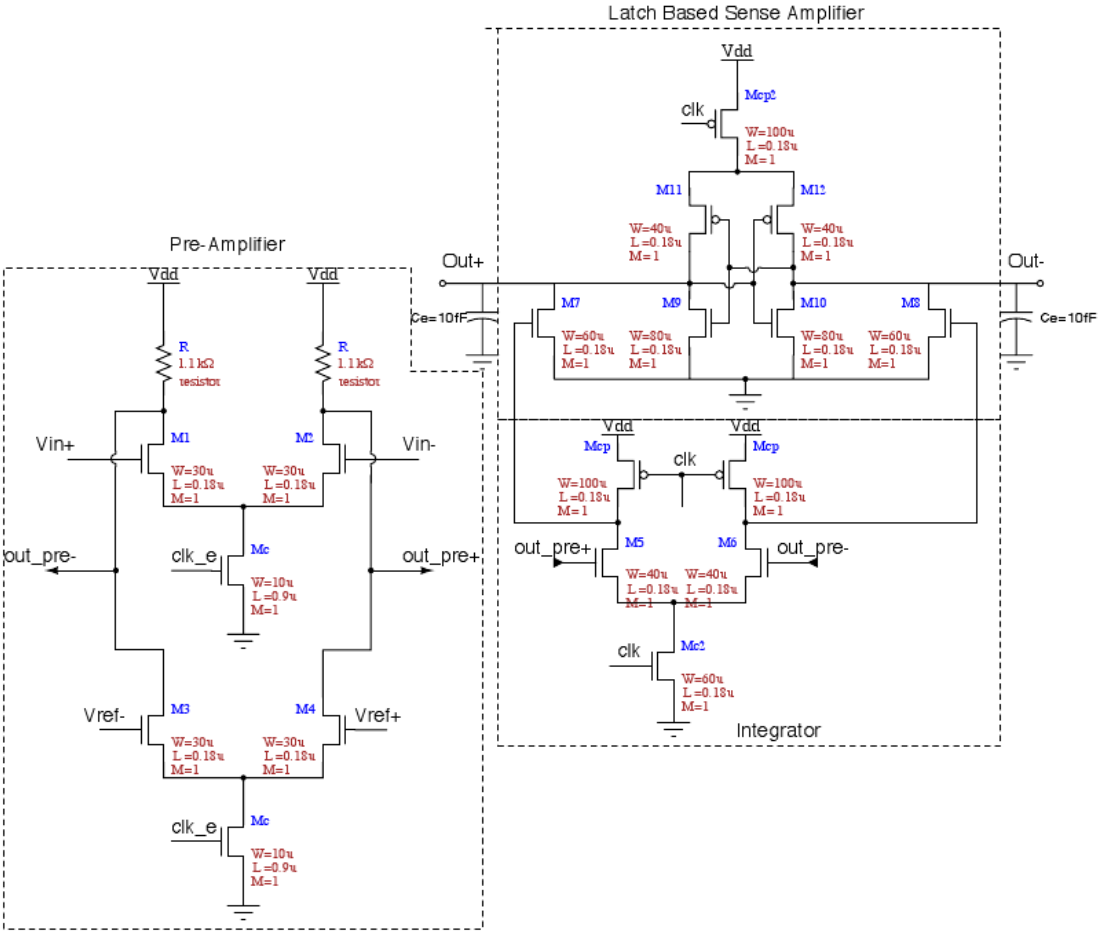

Fig. A3. Comparator Circuit

MATLAB Monte Carlo Simulations for the A/D Converter

σ(DNL) = 0.2 LSB (Specifications)
for 95% Yield, DNL specs should be <3*σ(DNL) = 0.6 LSB

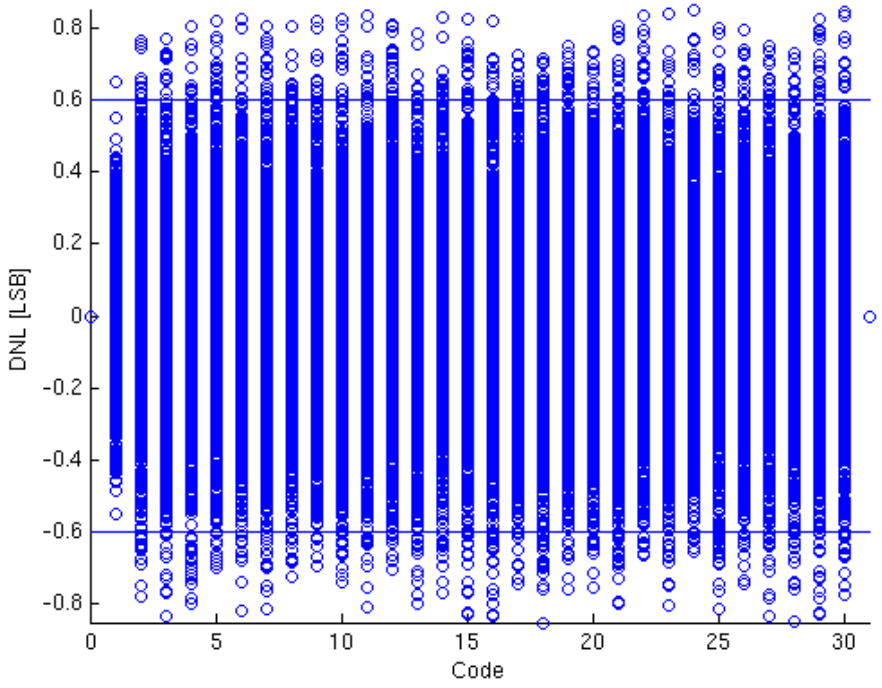

Fig. A4. Matlab ADC Monte Carlo DNL Simulation

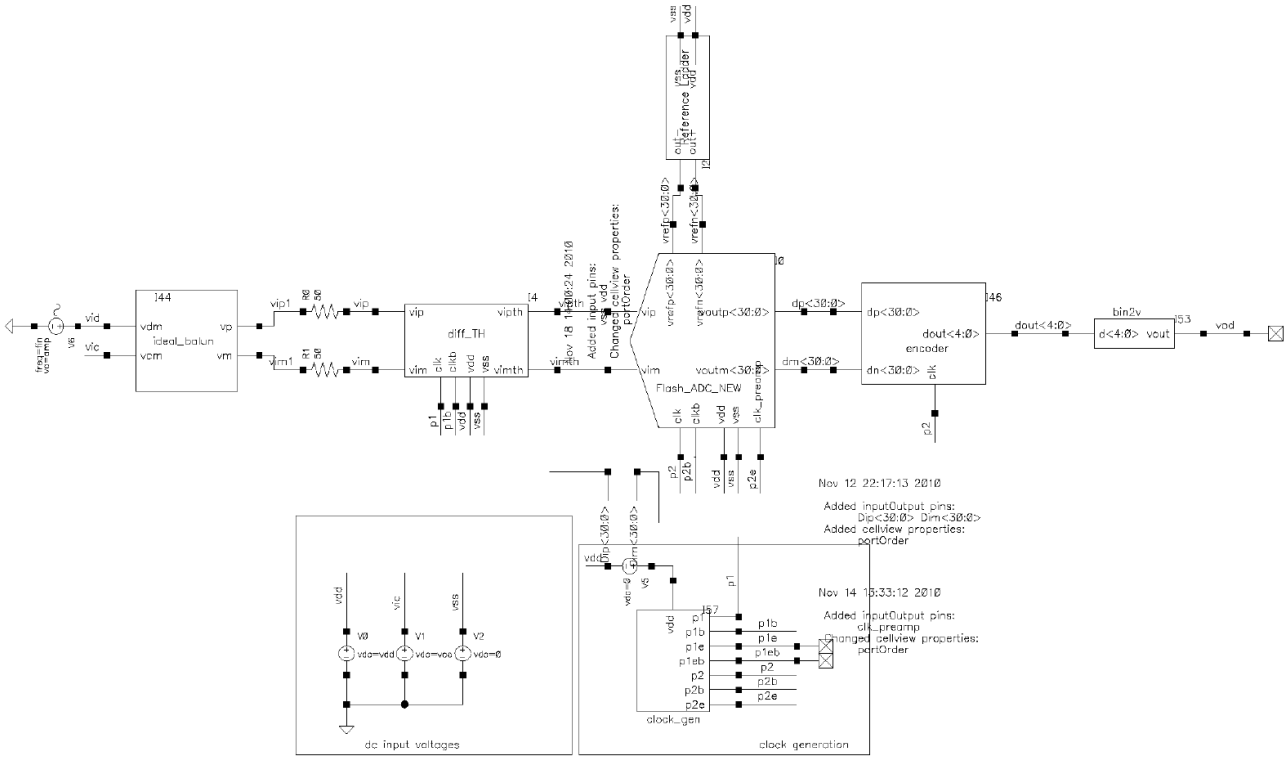

Fig. A5. Complete System Architecture

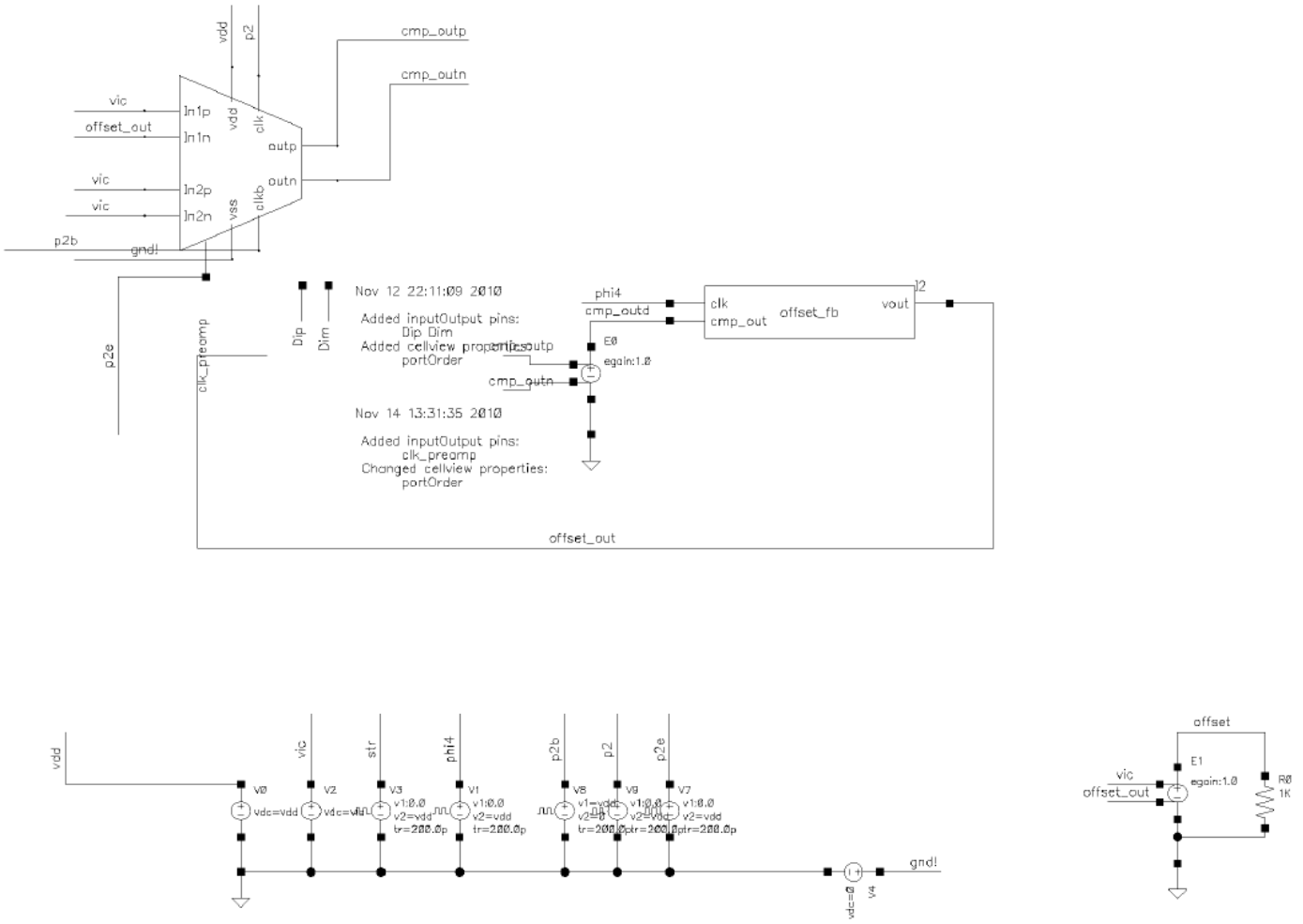

Fig. A6. Test Bench for Monte Carlo Analysis for Vt Mismatch