Fall - 2009

EE114 - Design Project

Differential Amplifier Design

Submitted by

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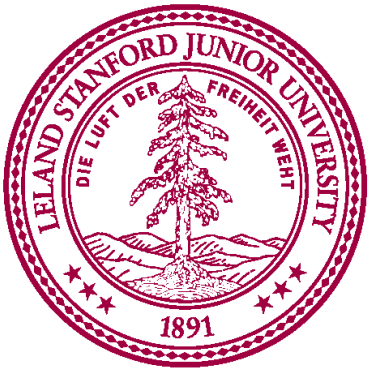


1. Design Abstract

The design flow started with the detailed analysis of an equivalent differential and common mode half circuit analysis of the given topology. Equations were identified determining various parameters; the two most important being gain and bandwidth. Utilizing these equations with additional constraints for other specifications (common mode output voltage), a matlab script was written to iterate over various design parameters meeting all the given specifications for the minimum power consumption. These values were simulated in hspice, and final optimization was done through a thoughtful fine tuning of values.

1.1 Design Flow

With the given differential architecture, the amplifier design has a total of 13 variables: width of each transistors (W1 – W5), length of each transistors (L1 – L5), R_s, R_L and I_{tail}. From previous experience in the course, the length of all transistors was kept to the minimum value (L_{min} = 1um) initially for minimizing power & current consumption for given specifications. By ratio metric scaling, $\frac{W_5}{W_4} = \frac{R_S}{R_L} = m$. Furthermore, it is observed that M3 and M2 form a current mirror, so the ratio of W_3 and W_2 will be determined by: $\frac{W_3}{W_2} = K$ .This leaves us with 5 design variables to optimize: W_1, W_2, W_4, K, and m.

The analysis was initially simplified under suitable assumptions to determine rough estimate of parameters. Matlab script (see Appendix) was compiled and simulated using the simplified equations and all the design constraints ($V_{o,cm}$, V_{ov}) to obtain a good estimate of all parameters. Once an initial design could be verified in hspice, more detailed analysis was done to estimate the error in the results, and verifying the assumptions.

Initial designs were done with an ideal current source with some R_{tail} to account for the practical input resistances. To satisfy the CMRR constraints (CMRR > 80db), the R_{tail} required was much higher (Detailed expression of CMRR in later section). Initially, R_{tail} was assumed to be of the order of 10^8 Ω. Furthermore, we knew that extra power would be burned in the non-ideal current source; an estimated scaling factor of 9-10 could easily be accounted for in the matlab script. Considerations for the current source design included a necessary high output resistance, along with low voltage overhead for higher voltage swing. Extra attention was paid to biasing the current source; a resistive divider is not optimal because it wastes power. A NMOS diode model was used to bias for minimum current overhead. Also, a large current scaling ratio (k <10) within the current source is also desired to minimize power.

Following the power optimized results from matlab, and using the proposed current source design, the entire differential circuit was simulated in hspice. The parameters were fine tuned to obtain the desired specifications and minimum power consumption. Whatever discrepancies between final values and matlab optimized results were minimal and could be traced back to our initial assumptions.

2. Design Details

2. 1 Design Analysis

Half –circuit analysis for the differential and common mode design has been done to determine tradeoffs between the parameter.

2.1.1 Gain Analysis

Constraint: $A_v \geq 10\ i.e. A_v\ \geq 20db$

While examining the half circuit of the differential amplifier, there are three stages which contribute to small signal gain.

1. Common Gate: V_{in} driving a small signal current: $I_1 \cong gm_1 * V_{in}$ through M1, which flows through M2.
2. Current Mirror: M2 & M3 is a recognized current mirror with current scaling ratio: $I_3 = \frac{W_3}{W_2} * I_2$.
3. Common Drain: $V_{out} = I_5 * R_L$, where I_5 is determined by the gate voltage at M5: $V_{g5} = I_3 * R_{in4}$ where R_{in4} is the impedance looking into the drain of M4.

Combining the gain through all the three stages, we calculate gain (A_v) as,

$$\text{Gain, } Av = \frac{v_o}{v_{in}} = \frac{gm5}{gm5+\frac{1}{RL_{tot}}} * R' * K * gm1$$

Where, $R' = [(\frac{1}{gm4})//ro4] * (1 + \frac{Rs}{(\frac{1}{gm4})//ro4} + gmb4 * Rs)$, and $RL_{tot} = RL//(\frac{1}{gmb5})//ro5$

This, equation can be simplified down under suitable assumptions to:

$$\boldsymbol{Av \approx Rs * K * gm1}$$

With design constraint Av > 10, and $gm = \sqrt{2 * I_d * Kp * \frac{W}{L}}$, the above eq. sets a restriction on Id1 as:

$$I_{d1} = \frac{\left(\frac{10}{Rs * K}\right)^2}{(Kp * \frac{W1}{L1})}$$

2.1.2 Power Analysis

Constraint: $P_{tot} < 1mW$

The design goal is to minimize power consumption. For half-circuit design it is given by:

$$P_1 = Vdd * (Id1 + Id3 + Id5)$$

The total power consumed by the differential amplifier is twice of the power consumed by the half circuit. To account for the power overhead because of the proposed current source design (scaling factor ~9), biasing current of the current source can be written as,

$$I_{bias} \approx 0.11 * I_{tail} \approx 0.11 * 2 * I_{d1}$$

As a result, total Power consumption of the design is given by,

$$P_{tot} = 2 * (1.11 * I_{d1} + I_{d3} + I_{d5})$$

Where, $Id3 = K * Id1$ *and* $Id5 = m * Id4 = m * Id3 = m * K * Id1$

2.1.3 Bandwidth Analysis

Constraint: $f_{3db} \geq 20MHz$

Bandwidth is estimated using the ZVTC analysis and determining the contributions from each intrinsic and extrinsic capacitance as well as determining the time constants at each node of the half circuit. Results obtained from detailed analysis are as follow:

$R_\alpha = \left(\frac{1}{gm4}\right)||ro4$, $R' = R_\alpha(1 + \frac{Rs}{R_\alpha} + gmb4 * Rs)$, $R'' = R'||ro3$, $a = \left(\frac{1}{gm2}\right)||ro1||ro2, b = \left(\frac{1}{gm2}\right)||ro2$, $Rx = ro3||R''$

At Input Node

$\tau 1 = Cgs1 * \frac{Ri}{2}$

$\tau 1' = Cgd1 * \left[\frac{Ri}{2} + a + gm1 * a * \frac{Ri}{2}\right]$

Assumptions in MATLAB simulations:
$C_{db}/C_{gs} \approx 0.33$
$C_{gd}/C_{gs} \approx 0.25$
$g_{mb}/g_m \approx 0.2$

At Node X

$\tau 2 = a * (Cdb1 + Cgs1 + Cdb2 + Cgs3)$

$\tau 3 = Cgd3 * (R'' + b + gm3 * R'' * b)$

At node Y

$\tau 3' = Rx * (Cdb3 + Cgd5 + Cdb4)$

At Output Node

$$\tau 4 = CL * \frac{1}{gm5 + \frac{1}{RL} + \frac{1}{ro5}}$$

$$\tau 4' = Cgs5 * \frac{\left[RL + Rx * \left(1 + gmb5 * RL + \frac{RL}{ro5}\right)\right]}{1 + gm5 * RL}$$

$$f_{-3db} = \frac{1}{2 * \pi} * \frac{1}{\tau 1 + \tau 1' + \tau 2 + \tau 3 + \tau 3' + \tau 4 + \tau 4'}$$

Observation: Note that $\tau 4$, $\tau 3'$ & $\tau 3$ are large values which effectively determine the bandwidth of the design. It puts a limit to the value of RL and size of M_{3A} (W_{3A}) which will be useful while analyzing the design and various tradeoffs.

2.1.4 Common Mode Analysis

Constraint: $2 \leq V_{cm,out} \leq 3$

The common mode output voltage is given by,

$V_{cm,out} = Id5 * RL = Id4 * Rs$

2.1.5 CMRR Analysis

Constraint: $CMRR \geq 80db$ (at low frequencies)

Using Differential Mode Half- Circuit Analysis (see 1.1),

$$A_{dm} = \frac{v_o}{v_{in}} = \frac{gm5}{gm5 + \frac{1}{RL_{tot}}} * R' * K * gm1$$

Using Common Mode Half- Circuit Analysis,

$$A_{cm} = \frac{v_{o\,cm}}{v_{i_{cm}}} = \frac{gm5}{gm5 + \frac{1}{RL_{tot}}} * R' * K * gm1 * \frac{r_{o1}}{[2 * R_{tail} + [1 + (g_{m1} + g_{mb1}) * 2 * R_{tail}] * r_{o1}]}$$

Hence, CMRR is given by,

$$CMRR = \frac{A_{dm}}{A_{cm}} = \frac{[2*R_{tail} + [1+(g_{m1} + g_{mb1})*2*R_{tail}]*r_{o1}]}{r_{o1}}$$

Other Constraints: $V_{ov_{(1-5)}} \geq 150\ mV$

All overdrive voltages must be ≥ 150 mV. Transconductances and V_{ov} are given by:

$V_{ov} = \sqrt{2 * \frac{Id}{Kp * \frac{W}{L}}}$ *and* $gm = 2 * \frac{Id}{Vov}$

2.2 Current Source Design

There are two important factors in choosing a current source. It must have a high input resistance (possibly cascode design), and low V_{omin} (voltage overhead). This ensures enough headroom for voltage swing. While several different topologies provide the same V_{omin}, the optimal current source wastes the least amount of power. We choose to use the magic battery topology from Lecture 3 slide21; because it has the minimum V_{omin} of $2V_{ov}$ and it only has one extra branch of wasted current (minimizes power).

Lot of thought has been given to the biasing circuit design for the current source and NMOS diode with minimum width (Wmin = 2um) and maximum length (Lmin = 50um) has been used to provide minimum current to the current source, and high current scaling was used to reduce power consumption. A Scaling factor (~7-9) has been used to optimize the design and provide the right bias current. The length and width values have been tweaked to get all transistors in saturation.

2.3 Optimization Strategy

Equations derived for Gain, bandwidth, Power, CMRR gives us the insight of trade-off between different parameters. Strategy followed for minimizing power while meeting all specs and constraints: sweep the five variables over a range to achieve gain spec; at each sweep, all relevant capacitances and resistances are calculated to ensure bandwidth constraints; power is calculated and is minimized, while maintaining all other constraints.

Biasing current (> 10um) and common mode output voltage (2-3v) constraints put a minimum limit over k & Rs. Bandwidth restrictions put a limit over RL which in turns limits Rs and m. Minimizing power limits the value of biasing current, which in turns effect the common mode output voltage & RL, Rs, m. Gain through CS stage (M1) cannot be made very large by increasing size of M2 because then, it increases the contribution of node-X in the bandwidth and reduces it.

Objective: A design objective was to try to keep common mode output voltage close to 2volts, so that gain of 10 could be achieved with 0.1v input voltage without resulting in clipping; this also results in minimizing I4*Rs, which minimizes power while keeping others parameters constant. Hence, RL values were kept in a range to satisfy both bandwidth & V_o(dc). Transistors sizing were kept in a reasonably

small range so that no single transistor end up doing most of the work. Increasing current scaling, k results in higher power but lower value of Rs required for vo(dc). CMRR could be achieved with very high R_{tail} (100 MegΩ) using cascaded current design.

3. Simulations Results

3.1 MATLAB Results

Matlab generated the following optimal design values for half-circuit:

W1	W2	W5	K	m	Rs	Id1	Power	-3dB BW
2.8um	2um	13um	1.2	2.25	148kΩ	11.3uA	277uW	20.00 MHz

L1 = L2 = L3 = L4 = L5 = 1um

Remark: Value of L = Lmin has been obtained from the Matlab analysis i.e. it justifies our initial assumption that the minimum power for given design can be obtained only at the minimum values of L.

These numbers were generated for a half circuit, so total estimated bias current is 22.6uA and power consumption 554uW.

With these numbers, a fully differential circuit was simulated in hspice with the designed current source (see below) to verify specs. This first pass design yield:

3.2 Spice Results with MATLAB Values

Gain (A_v)	Bandwidth (f_{3db})	Power (P_{tot})
18.7dB	19.9 MHz	576uW

Observation: The gain obtained is a bit lower than the desired values because of our simplification of the gain expression. The power consumption in spice results is higher because current consumption due to practical current source is also taken into account. These discrepancies are further discussed in *3.4*.

3.3 Final HSPICE Optimizations

We noticed from the first pass simulation that the gain (A_v) was insufficient. Gain is given by:

$$Av \approx Rs * K * gm1$$

All three parameters, gm1, Rs, and K, can be tweaked to increase gain. By experimenting with these parameters in hspice, we were able to determine the tradeoffs of trying to increase gain and effect on other constraints.

if K increases	if Rs increases	if g_{m1} increases
Power (P_{tot}) Increases	Bandwidth (f_{3db}) reduces	Not much impact on Power or BW

Observations: We determined that increasing gm1, has little effect on power consumption (set by currents), and little effect on the bandwidth. Gm1 became the best "knob" to tweak to increase gain. To increase g_{m1}, only W1 in increased and not Id1 (because if Id1 increases then power increases and difficult to meet other constraints). The additional parameters were tweaked slightly to further reduce power and meet bandwidth specs.

3.4 Comparison between hand calculation and spice results

	Calculations	Spice with Matlab Values	Spice after optimization
Gain	20dB	18.9dB	20.709dB
Bandwidth	20.00 MHz	19.9MHz	20.015MHz
CMRR	102dB	87.47dB	89.67dB
Power	554uW	576uW	575uW

Hand calculations are the values obtained from our Matlab script. We see that most values from spice match within a few percent error. The largest margin was in CMRR, where we assumed the input resistance to the current source to be 100 MΩ. Another discrepancy was the lower gain obtained in spice. The simplified expression for gain neglected the common drain stage which slightly reduces gain by $(\frac{gm5}{gm5+\frac{1}{RL_{tot}}})$. In the bandwidth calculation, we neglected source to body capacitances which had little effect. The only other real discrepancy is in the power consumed. This was mainly due to the non-ideal current source used in spice, as well as increase drain currents due to channel length modulation.

3.5 Final Design Parameters

Given Parameters:

Vdd	5 V
C_L	1 pF
R_i	10 kΩ
V_{id}	200 mV (p-to-p)
V_{ic} (dc)	1.5 V – 3.5 V

Amplifier Design Parameters:

W_{1A}, W_{1B}	4.6 um
W_{2A}, W_{2B}	2.0 um
W_{3A}, W_{3B}	2.4 um
W_{4A}, W_{4B}	5.4 um
W_{5A}, W_{5B}	12.4 um

L_{1A}, L_{1B}	1 um
L_{2A}, L_{2B}	1 um
L_{3A}, L_{3B}	1 um
L_{4A}, L_{4B}	1 um
L_{5A}, L_{5B}	1 um

R_{SA}, R_{SB}	144 kΩ
R_{LA}, R_{LB}	64 kΩ
I_bias	21.9 uA

Current Source Design Parameters:

W_{CB}	2.0 um
W_{C1}	5.0 um
W_{C2}	2.0 um
W_{C3}, W_{C4}	2.0 um
W_{C5}, W_{C6}	17 um

L_{CB}	50 um
L_{C1}	5.0 um
L_{C1}	10 um
L_{C3}, L_{C6}	2.0 um
L_{C4}, L_{C5}	2.0 um

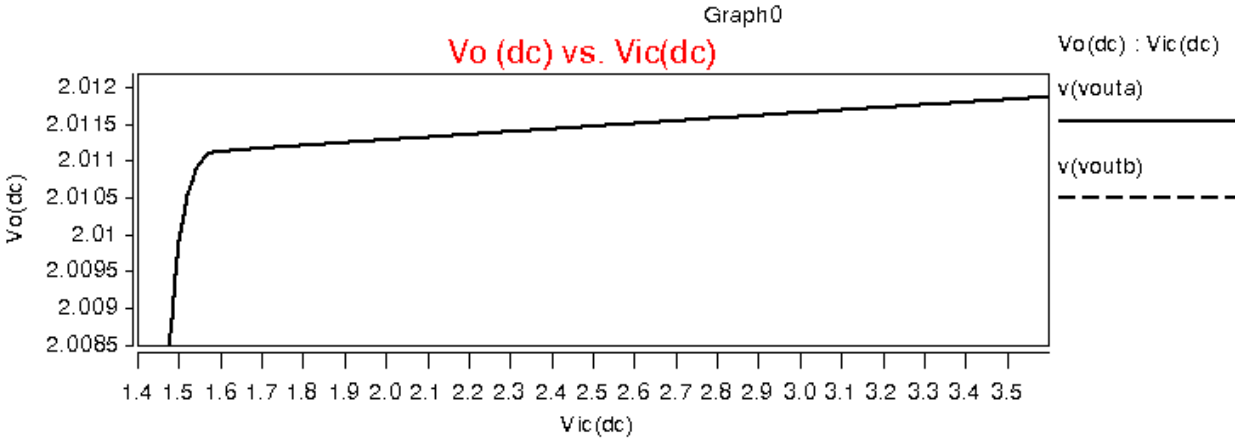
3.6 Final Spice Results

Parameter	SPICE Results
Small Signal Voltage Gain, $\mathbf{A_v}$ **(V_{od}/V_{id})**	**20.709 db**
Bandwidth, $\mathbf{f_{3db}}$	**20.015 MHz**
Common Mode Output Voltage, **Vo (dc)**	**~ 2.01 V**
Common Mode Rejection Ratio, **CMRR**	**89.67 db** (at low frequency)
Total Power Dissipation, $\mathbf{P_{tot}}$	**574.94 W**

3.7 Final Plots

3.7.1 Common Mode Output Voltage (Vo(dc)) vs. Common Mode Input Voltage (Vic(dc))

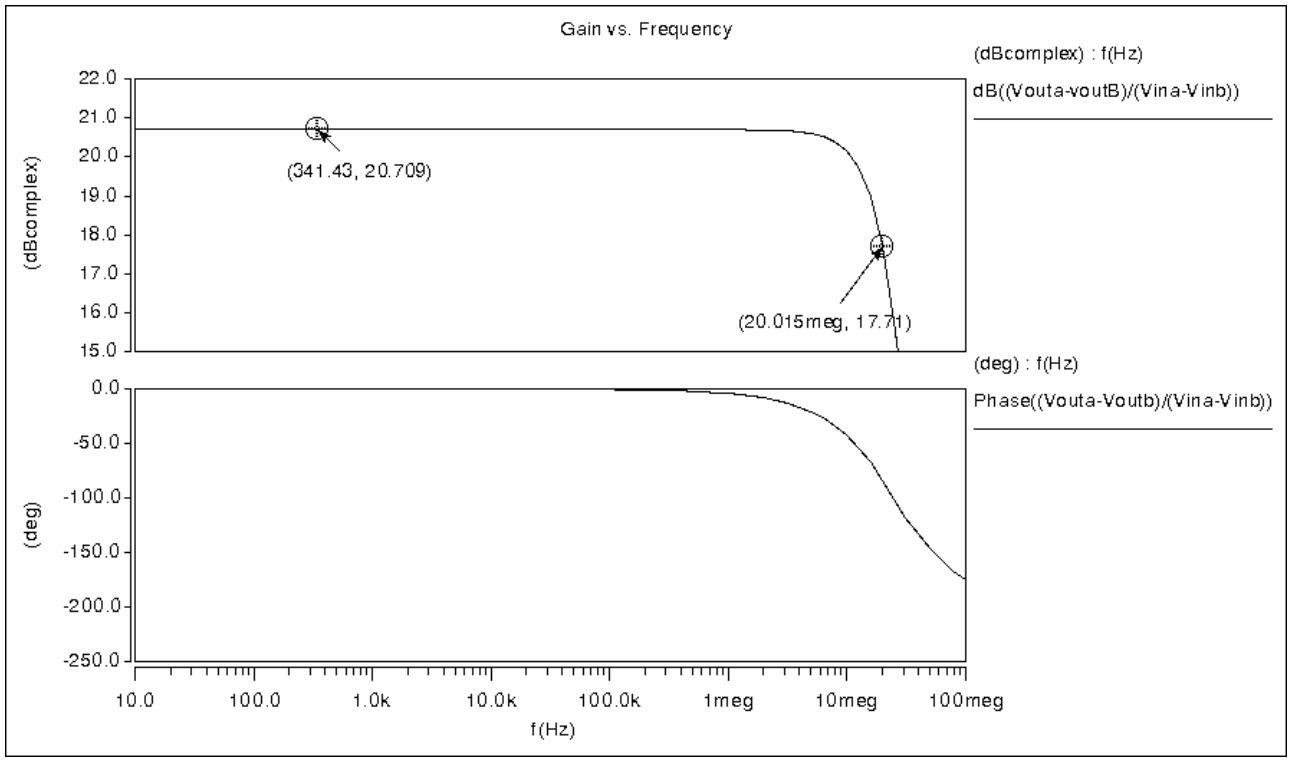
Vo(dc) ≈ 2.01 Volts



3.7.2 Gain vs. Frequency

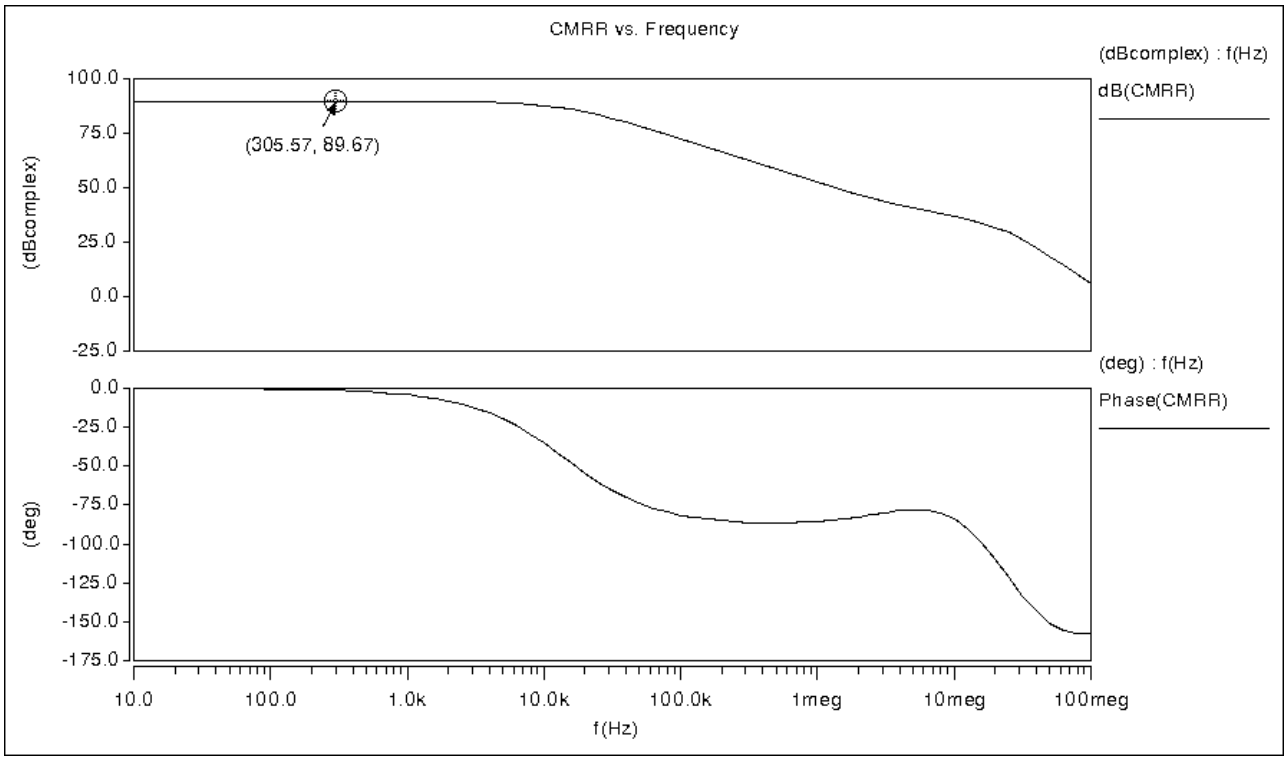
A_v = 20.709 db

f_{3db} = 20.015 db



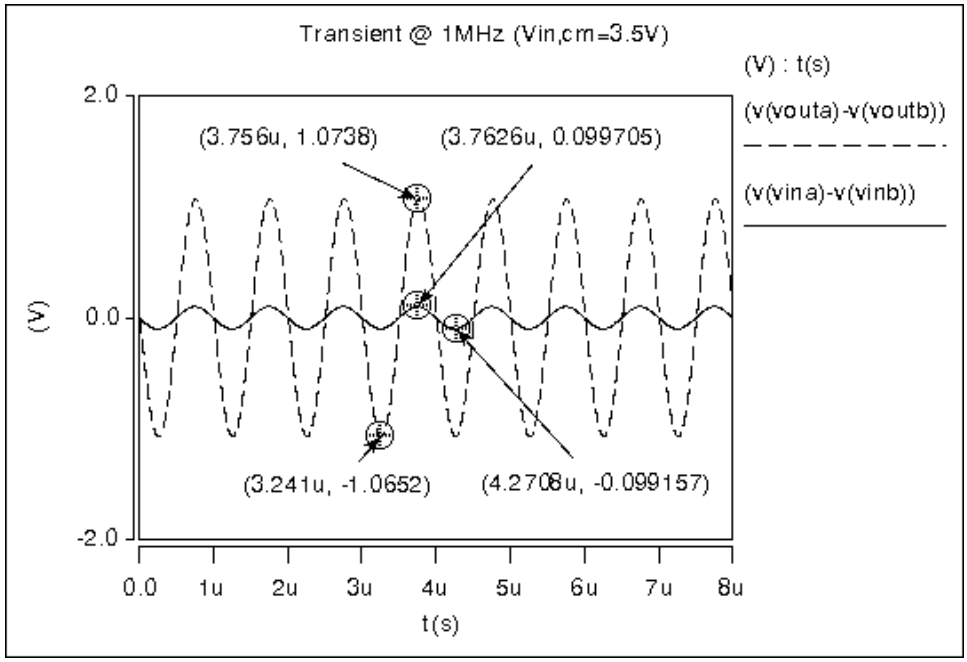
3.7.2 CMRR vs. Frequency

CMRR = 89.67 db (at low frequency)



6.3.4 Transient Analysis

Vin (p-to-p) = 200mV
Vout (p-to-p) = 2.13 V
Gain, Av ≈ 20.54 dB



4. Conclusions

In this project, we were able to successfully design a differential amplifier within the given specifications. While the design was sufficient for the class, we noticed that the significant distortion occurred at higher frequencies. These high frequency distortions could be the result of low CMRR at high frequencies and due to high frequency second order distortions which were neglected in the model of transistor assumed. These frequency distortions are assumed to be taken care of by filters. However, 20MHz is certainly not considered “high” in modern day communications. Additional thought must be put into designing power amplifiers for high frequencies.

The project gave an insight of approach to be followed while analyzing a large circuit with lot many parameters. The project gave a firsthand experience of determining the various tradeoffs within a circuit and ways to reduce and make suitable assumptions to estimate parameters like power, bandwidth, and current of the design.

The PVT analysis has not been done for the design due to lack of time, which is an inevitable step to make more robust design.

5. Feedback

Working over the given project was really good experience. It would have been better if some flexibility to play with the architecture of the amplifier would have been given. Project should be given a week or so earlier to give more time to try different architectures for the design.

6. Appendix

Appendix A: HSPICE Code

```
* Design Project: EE114
.include ee114_hspice.sp

*********  Differential Amplifier  ****************
m1A XA vinA d1A 0 nmos114 w=4.6u l=1u
m2A XA XA vdd vdd pmos114 w=2u l=1u
m3A YA XA vdd vdd pmos114 w=2.4u l=1u
m4A YA YA s4A 0 nmos114 w=5.4u l=1u
RSA s4A 0 144k
m5A vdd YA voutA 0 nmos114 w=12.4u l=1u
RLA voutA 0 64k

m1B XB vinB d1A 0 nmos114 w=4.6u l=1u
m2B XB XB vdd vdd pmos114 w=2u l=1u
m3B YB XB vdd vdd pmos114 w=2.4u l=1u
m4B YB YB s4B 0 nmos114 w=5.4u l=1u
RSB s4B 0 144k
m5B vdd YB voutB 0 nmos114 w=12.4u l=1u
RLB voutB 0 64k
**********************************************

*********  Current Source  *********************
MCB1 vdd vdd vmagic 0 nmos114 w=2u l=50u
MC1 vmagic vmagic vds 0 nmos114 w=5u l=5u
MC2 vds vmagic d3 0 nmos114 w=2u l=10u

MC3 d3 vds s3 0 nmos114 w=2u l=2u
MC4 s3 d3 0 0 nmos114 w=2u l=2u
MC5 d5 d3 0 0 nmos114 w=17u l=2u
MC6 d1A vds d5 0 nmos114 w=17u l=2u
**********************************************
CL voutA voutB 1p
RiA vinA vidA 5k
RiB vinB vidB 5k

*********  Differential Voltage  *****************
*for Transient Analysis
*vid1 cm vidA SIN(0 0.1 1000k 0 0 0)
*vid2 cm vidB SIN(0 0.1 1000k 0 0 180)

vid1 cm vidA ac 0.1
vid2 vidB cm ac 0.1

** To do common mode analysis
*vid2 cm vidB ac 0.1

vcm1 cm 0 dc 3.5
V1 vdd 0 5
**********************************************

.op
.option post brief nomod
.TF V(voutA,voutB) vid1
*.TRANS 0.0001u 20u
.dc vcm1 1.4 3.6 0.01
.ac dec 10 10 300meg
.end
```

Appendix B: SPICE Result

```
******  operating point information     tnom=  25.000 temp=  25.000
******
***** operating point status is all      simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage

+0:cm     =  3.5000  0:d1a    =  2.2102  0:d3     = 818.1748m
+0:d5     = 326.4294m 0:s3     = 318.5414m 0:s4a    =  1.9930
+0:s4b    =  1.9930  0:vdd    =  5.0000  0:vds    =  1.2332
+0:vida   =  3.5000  0:vidb   =  3.5000  0:vina   =  3.5000
+0:vinb   =  3.5000  0:vmagic =  2.3692  0:vouta  =  2.0118
+0:voutb  =  2.0118  0:xa     =  3.8731  0:xb     =  3.8731
+0:ya     =  3.2607  0:yb     =  3.2607


****  voltage sources

subckt
element  0:vid1    0:vid2    0:vcm1    0:v1
 volts     0.        0.        3.5000    5.0000
 current   0.        0.        0.     -114.9849u
 power     0.        0.        0.      574.9244u


   total voltage source power dissipation=  574.9244u       watts

**** resistors

subckt
element  0:rsa     0:rla     0:rsb     0:rlb     0:ria     0:rib
 r value  144.0000k   64.0000k  144.0000k   64.0000k    5.0000k    5.0000k
 v drop    1.9930    2.0118    1.9930    2.0118    0.        0.
 current   13.8402u   31.4348u   13.8402u   31.4348u   0.        0.
 power     27.5833u   63.2416u   27.5833u   63.2416u   0.        0.



**** mosfets


subckt
element  0:m1a     0:m2a     0:m3a     0:m4a     0:m5a     0:m1b
model    0:nmos114. 0:pmos114. 0:pmos114. 0:nmos114. 0:nmos114. 0:nmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id       10.9318u  -10.9318u  -13.8402u   13.8402u   31.4348u   10.9318u
 ibs     -22.1017f    0.        0.       -19.9298f  -20.1183f  -22.1017f
 ibd     -38.7311f   11.2689f   17.3930f  -32.6070f  -50.0000f  -38.7311f
 vgs       1.2898   -1.1269   -1.1269    1.2677    1.2489    1.2898
 vds       1.6629   -1.1269   -1.7393    1.2677    2.9882    1.6629
 vbs      -2.2102    0.        0.       -1.9930   -2.0118   -2.2102
 vth       1.0043  -500.0000m -500.0000m  966.0772m  969.4544m    1.0043
 vdsat    285.4913m -626.8867m -626.8867m  301.6379m  279.4157m  285.4913m
 vod      285.4913m -626.8867m -626.8867m  301.6379m  279.4157m  285.4913m
 beta     268.2476u   55.6344u   70.4358u  304.2283u  805.2665u  268.2476u
 gam eff  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm        76.5824u   34.8765u   44.1553u   91.7668u  225.0041u   76.5824u
 gds      937.3108n  982.4673n    1.1790u    1.2283u    2.4203u  937.3108n
 gmb       13.2420u   11.6979u   14.8101u   16.4730u   40.2548u   13.2420u
 cdtot      6.0364f    4.3873f    4.5821f    6.9778f   12.8217f    6.0364f
 cgtot     11.7789f    5.1093f    6.1357f   13.8186f   31.8162f   11.7789f
```

cstot	13.6747f	8.6667f	9.9800f	15.8253f	33.6418f	13.6747f
cbtot	8.1363f	8.0161f	8.5122f	9.2196f	15.2255f	8.1363f
cgs	9.3534f	4.0667f	4.8800f	10.9800f	25.2134f	9.3534f
cgd	2.3235f	1.0069f	1.2128f	2.7210f	6.3136f	2.3235f

subckt						
element	0:m2b	0:m3b	0:m4b	0:m5b	0:mcb1	0:mc1
model	0:pmos114.	0:pmos114.	0:nmos114.	0:nmos114.	0:nmos114.	0:nmos114.
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-10.9318u	-13.8402u	13.8402u	31.4348u	2.5712u	2.5712u
ibs	0.	0.	-19.9298f	-20.1183f	-23.6922f	-12.3322f
ibd	11.2689f	17.3930f	-32.6070f	-50.0000f	-50.0000f	-23.6922f
vgs	-1.1269	-1.1269	1.2677	1.2489	2.6308	1.1360
vds	-1.1269	-1.7393	1.2677	2.9882	2.6308	1.1360
vbs	0.	0.	-1.9930	-2.0118	-2.3692	-1.2332
vth	-500.0000m	-500.0000m	966.0772m	969.4544m	1.0315	818.8894m
vdsat	-626.8867m	-626.8867m	301.6379m	279.4157m	1.5993	317.1166m
vod	**-626.8867m**	**-626.8867m**	**301.6379m**	**279.4157m**	**1.5993**	**317.1166m**
beta	55.6344u	70.4358u	304.2283u	805.2665u	2.0105u	51.1360u
gam eff	600.0000m	600.0000m	600.0000m	600.0000m	600.0000m	600.0000m
gm	34.8765u	44.1553u	91.7668u	225.0041u	3.2154u	16.2161u
gds	982.4673n	1.1790u	1.2283u	2.4203u	5.1155n	50.2815n
gmb	11.6979u	14.8101u	16.4730u	40.2548u	541.8536n	3.4117u
cdtot	4.3873f	4.5821f	6.9778f	12.8217f	4.2298f	7.0293f
cgtot	5.1093f	6.1357f	13.8186f	31.8162f	156.5506f	44.0136f
cstot	8.6667f	9.9800f	15.8253f	33.6418f	157.3022f	46.0024f
cbtot	8.0161f	8.5122f	9.2196f	15.2255f	5.8008f	10.2040f
cgs	4.0667f	4.8800f	10.9800f	25.2134f	154.3341f	40.8335f
cgd	1.0069f	1.2128f	2.7210f	6.3136f	1.8068f	2.5871f

subckt					
element	0:mc2	0:mc3	0:mc4	0:mc5	0:mc6
model	0:nmos114.	0:nmos114.	0:nmos114.	0:nmos114.	0:nmos114.
region	Linear	Saturati	Saturati	Saturati	Saturati
id	2.5712u	2.5712u	2.5712u	21.8636u	21.8636u
ibs	-8.1817f	-3.1854f	0.	0.	-3.2643f
ibd	-12.3322f	-8.1817f	-3.1854f	-3.2643f	-22.1017f
vgs	1.5510	914.6767m	818.1748m	818.1748m	906.7887m
vds	415.0433m	499.6334m	318.5414m	326.4294m	1.8837
vbs	-818.1748m	-318.5414m	0.	0.	-326.4294m
vth	726.5887m	597.9104m	500.0000m	500.0000m	600.1440m
vdsat	415.0433m	316.7663m	318.1748m	318.1748m	306.6447m
vod	**824.4607m**	**316.7663m**	**318.1748m**	**318.1748m**	**306.6447m**
beta	10.0415u	51.2491u	50.7964u	431.9366u	465.0296u
gam eff	600.0000m	600.0000m	600.0000m	600.0000m	600.0000m
gm	4.1677u	16.2340u	16.1621u	137.4313u	142.5989u
gds	4.1368u	125.4261n	126.5440n	1.0756u	999.0792n
gmb	982.8806n	4.6049u	5.4209u	46.0959u	40.3074u
cdtot	21.4102f	4.7045f	5.1591f	23.3658f	19.2273f
cgtot	46.4732f	8.2602f	8.2739f	70.3292f	70.3852f
cstot	31.9888f	11.2885f	11.7334f	77.2336f	75.4654f
cbtot	7.3416f	7.9743f	8.8918f	32.5934f	26.4179f
cgs	28.2904f	7.1334f	7.1334f	60.6336f	60.6336f
cgd	17.9749f	1.0061f	1.0039f	8.5340f	8.6964f

Appendix D: Gain variation w.r.t common Mode Input Voltage

vcm1	input resistance at vid1	output resistance at v(vouta,vo	v(vouta,voutb)/vid1
1.4000	1.000e+20	7.0781k	-11.6510
1.5000	1.000e+20	7.0619k	-11.6248
1.6000	1.000e+20	7.0604k	-11.5894
1.7000	1.000e+20	7.0604k	-11.5530
1.8000	1.000e+20	7.0603k	-11.5162
1.9000	1.000e+20	7.0603k	-11.4791
2.0000	1.000e+20	7.0602k	-11.4418
2.1000	1.000e+20	7.0602k	-11.4042
2.2000	1.000e+20	7.0601k	-11.3663
2.3000	1.000e+20	7.0601k	-11.3281
2.4000	1.000e+20	7.0600k	-11.2897
2.5000	1.000e+20	7.0600k	-11.2510
2.6000	1.000e+20	7.0600k	-11.2121
2.7000	1.000e+20	7.0599k	-11.1729
2.8000	1.000e+20	7.0599k	-11.1335
2.9000	1.000e+20	7.0598k	-11.0938
3.0000	1.000e+20	7.0598k	-11.0539
3.1000	1.000e+20	7.0597k	-11.0137
3.2000	1.000e+20	7.0597k	-10.9733
3.3000	1.000e+20	7.0596k	-10.9327
3.4000	1.000e+20	7.0596k	-10.8918
3.5000	1.000e+20	7.0596k	-10.8507
3.6000	1.000e+20	7.0595k	-10.8094